ST75320

320X240 Dot Matrix LCD Controller/Driver

Datasheet

Version 1.1

2015/07/14

Sitronix Technology Corporation

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1 introduction

ST75320 is a driver & controller LSI for mono graphic dot-matrix liquid crystal display systems. It incorporates power system, LCD controller and drivers for common/segment outputs. ST75320 can be connected directly to a microprocessor with 8-bit parallel interface, 4-line serial interface (SPI-4), 3-line serial interface (SPI-3) and I^2C interface. Display data sent from MCU is stored into internal Display Data RAM (DDRAM) of 320x240 bits. ST75320 contains 320 segment-output and 240 common-output. The display data bits in DDRAM are directly related to the pixels on LCD panel. With built-in oscillation circuit and power circuits, ST75320 can drive LCD panel without external clock or power, so that it is possible to make a display system with the fewest components.

2 FEATURES

Single-chip LCD controller/driver

Driver Output Circuits

- 320 segment outputs / 240 common outputs

On-chip Display Data RAM

- Capacity: 320 x 240 = 76800 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MCU
- 4-Line (8-bit) and 3-Line (9-bit) serial interfaces support write-operation and register-read (status/temperature…)
- I2C interface support write-operation and register-read (status/temperature…)
- All interfaces can read temperature (when sensor is ON), IC status and OTP data (register value)

External RSTB (Hardware Reset) Pin

On-chip Oscillator Circuit

- Internal oscillator requires no external component (external clock input is also supported)

On-chip Low Power Analog Circuit

- Built-in voltage regulator with programmable contrast
- Built-in OTP to optimize Vop for LCD panel Built-in voltage follower for LCD bias voltages
- Support external power supply

Display Function

- Duty: 1/32 ~ 1/240
- Support interlace-scanning method
- N-lines inversion

Built-in Temperature Sensor

- Temperature compensation with built-in thermal sensor
- Programmable Vop thermal gradient (19-slopes) and frame frequencies

Operating Voltage Range

- Digital Power (VDD1): 3V ~ 5.0V (TYP.)
- Analog Power (VDD2, VDD3): 3V ~ 5.0V (TYP.)

LCD Operating Voltage Range

- Maximum Vop: 33.0V (Vop = V3 - MV3)

Package Type: COG , COF

Only for Industrial Use

ST75320	**6800 , 8080 , 4-Line , 3-Line**	
ST75320i	**I^2C Interface**	

3 PAD ARRANGEMENT

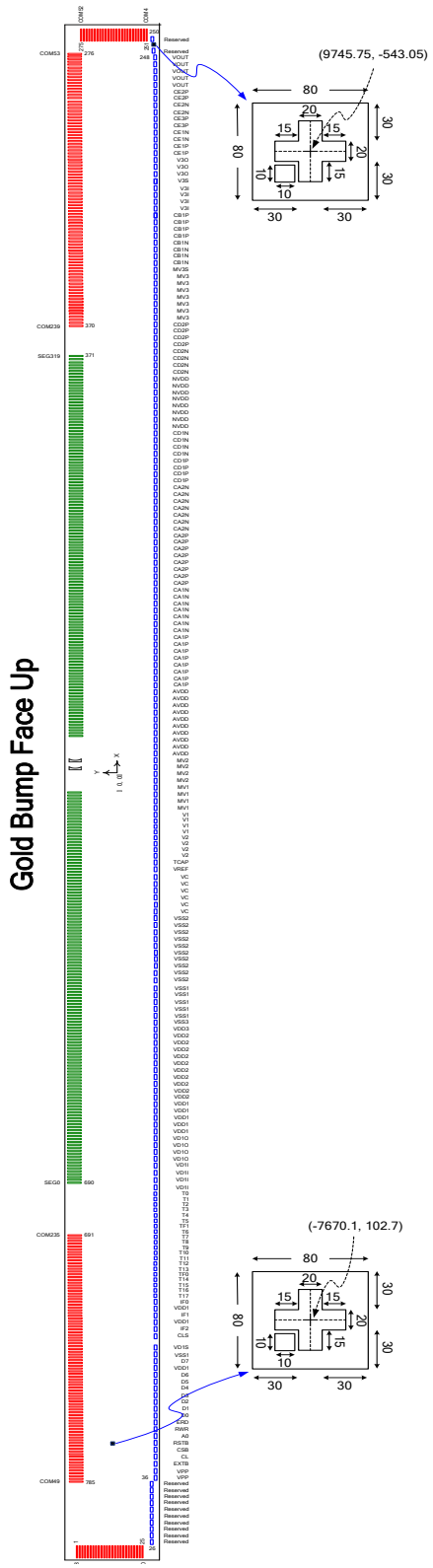


Figure 1 Chip Outline

ST75320			
Chip Size		20767x1287	
Chip Thickness	480	**Bump Height**	12
PAD No.		**Bump Size**	
1~25, 251~275		96 x 27	
36~61,82~248		62 x 45	
62~81		32 x 45	
276~370,691~785		27 x 96	
371~690		16 x 96	
26~35, 249~250		62 x 45	
PAD No.		**Bump Pitch**	
1~25, 251~275		45	
36~38,82~129,130~248		80	
38~41,44~51,52~53, 129~130		145	
41~44, 51~52, 53~61		125	
61~62		110	
62~81		50	
81~82		65	
276~370,691~785		45	
371~690		34	
26~36, 249~250		145	
* Refer to “PAD CENTER COORDINATES” for ITO layout			

Unit: um

4 PAD CENTER COORDINATES

PAD	NAME	X	Y
1	COM48	-10287	540
2	COM43	-10287	495
3	COM42	-10287	450
4	COM41	-10287	405
5	COM40	-10287	360
6	COM35	-10287	315
7	COM34	-10287	270
8	COM33	-10287	225
9	COM32	-10287	180
10	COM27	-10287	135
11	COM26	-10287	90
12	COM25	-10287	45
13	COM24	-10287	0
14	COM19	-10287	-45
15	COM18	-10287	-90
16	COM17	-10287	-135
17	COM16	-10287	-180
18	COM11	-10287	-225
19	COM10	-10287	-270
20	COM9	-10287	-315
21	COM8	-10287	-360
22	COM3	-10287	-405
23	COM2	-10287	-450
24	COM1	-10287	-495
25	COM0	-10287	-540
26	Reserved	-9832.6	-528.7
27	Reserved	-9557.8	-528.7
28	Reserved	-9412.8	-528.7
29	Reserved	-9267.8	-528.7
30	Reserved	-9122.8	-528.7
31	Reserved	-8977.8	-528.7

PAD	NAME	X	Y
32	Reserved	-8832.8	-528.7
33	Reserved	-8687.8	-528.7
34	Reserved	-8542.8	-528.7
35	Reserved	-8372.8	-569
36	VPP	-8227.8	-569
37	VPP	-8147.8	-569
38	EXTB	-8067.8	-569
39	CL	-7922.8	-569
40	CSB	-7777.8	-569
41	RSTB	-7632.8	-569
42	A0	-7507.8	-569
43	RWR	-7382.8	-569
44	ERD	-7257.8	-569
45	D0	-7112.8	-569
46	D1	-6967.8	-569
47	D2	-6822.8	-569
48	D3	-6677.8	-569
49	D4	-6532.8	-569
50	D5	-6387.8	-569
51	D6	-6242.8	-569
52	VDD1	-6117.8	-569
53	D7	-5972.8	-569
54	VSS1	-5847.8	-569
55	VD1S	-5722.8	-569
56	CLS	-5597.8	-569
57	IF2	-5472.8	-569
58	VDD1	-5347.8	-569
59	IF1	-5222.8	-569
60	VDD1	-5097.8	-569
61	IF0	-4972.8	-569
62	T17	-4862.8	-569

PAD	NAME	X	Y
63	T16	-4812.8	-569
64	T15	-4762.8	-569
65	T14	-4712.8	-569
66	TF0	-4662.8	-569
67	T13	-4612.8	-569
68	T12	-4562.8	-569
69	T11	-4512.8	-569
70	T10	-4462.8	-569
71	T9	-4412.8	-569
72	T8	-4362.8	-569
73	T7	-4312.8	-569
74	T6	-4262.8	-569
75	TF1	-4212.8	-569
76	T5	-4162.8	-569
77	T4	-4112.8	-569
78	T3	-4062.8	-569
79	T2	-4012.8	-569
80	T1	-3962.8	-569
81	T0	-3912.8	-569
82	VD1I	-3847.8	-569
83	VD1I	-3767.8	-569
84	VD1I	-3687.8	-569
85	VD1I	-3607.8	-569
86	VD1O	-3527.8	-569
87	VD1O	-3447.8	-569
88	VD1O	-3367.8	-569
89	VD1O	-3287.8	-569
90	VDD1	-3207.8	-569
91	VDD1	-3127.8	-569
92	VDD1	-3047.8	-569
93	VDD1	-2967.8	-569
94	VDD1	-2887.8	-569
95	VDD2	-2807.8	-569
96	VDD2	-2727.8	-569
97	VDD2	-2647.8	-569

PAD	NAME	X	Y
98	VDD2	-2567.8	-569
99	VDD2	-2487.8	-569
100	VDD2	-2407.8	-569
101	VDD2	-2327.8	-569
102	VDD2	-2247.8	-569
103	VDD2	-2167.8	-569
104	VDD2	-2087.8	-569
105	VDD3	-2007.8	-569
106	VSS3	-1927.8	-569
107	VSS1	-1847.8	-569
108	VSS1	-1767.8	-569
109	VSS1	-1687.8	-569
110	VSS1	-1607.8	-569
111	VSS1	-1527.8	-569
112	VSS2	-1447.8	-569
113	VSS2	-1367.8	-569
114	VSS2	-1287.8	-569
115	VSS2	-1207.8	-569
116	VSS2	-1127.8	-569
117	VSS2	-1047.8	-569
118	VSS2	-967.8	-569
119	VSS2	-887.8	-569
120	VSS2	-807.8	-569
121	VSS2	-727.8	-569
122	VC	-647.8	-569
123	VC	-567.8	-569
124	VC	-487.8	-569
125	VC	-407.8	-569
126	VC	-327.8	-569
127	VC	-247.8	-569
128	VREF	-167.8	-569
129	TCAP	-87.8	-569
130	V2	57.2	-569
131	V2	137.2	-569
132	V2	217.2	-569

PAD	NAME	X	Y
133	V2	297.2	-569
134	V1	377.2	-569
135	V1	457.2	-569
136	V1	537.2	-569
137	V1	617.2	-569
138	MV1	697.2	-569
139	MV1	777.2	-569
140	MV1	857.2	-569
141	MV1	937.2	-569
142	MV2	1017.2	-569
143	MV2	1097.2	-569
144	MV2	1177.2	-569
145	MV2	1257.2	-569
146	AVDD	1337.2	-569
147	AVDD	1417.2	-569
148	AVDD	1497.2	-569
149	AVDD	1577.2	-569
150	AVDD	1657.2	-569
151	AVDD	1737.2	-569
152	AVDD	1817.2	-569
153	AVDD	1897.2	-569
154	AVDD	1977.2	-569
155	AVDD	2057.2	-569
156	CA1P	2137.2	-569
157	CA1P	2217.2	-569
158	CA1P	2297.2	-569
159	CA1P	2377.2	-569
160	CA1P	2457.2	-569
161	CA1P	2537.2	-569
162	CA1P	2617.2	-569
163	CA1P	2697.2	-569
164	CA1N	2777.2	-569
165	CA1N	2857.2	-569
166	CA1N	2937.2	-569
167	CA1N	3017.2	-569

PAD	NAME	X	Y
168	CA1N	3097.2	-569
169	CA1N	3177.2	-569
170	CA1N	3257.2	-569
171	CA2P	3337.2	-569
172	CA2P	3417.2	-569
173	CA2P	3497.2	-569
174	CA2P	3577.2	-569
175	CA2P	3657.2	-569
176	CA2P	3737.2	-569
177	CA2P	3817.2	-569
178	CA2P	3897.2	-569
179	CA2N	3977.2	-569
180	CA2N	4057.2	-569
181	CA2N	4137.2	-569
182	CA2N	4217.2	-569
183	CA2N	4297.2	-569
184	CA2N	4377.2	-569
185	CA2N	4457.2	-569
186	CD1P	4537.2	-569
187	CD1P	4617.2	-569
188	CD1P	4697.2	-569
189	CD1P	4777.2	-569
190	CD1N	4857.2	-569
191	CD1N	4937.2	-569
192	CD1N	5017.2	-569
193	CD1N	5097.2	-569
194	NVDD	5177.2	-569
195	NVDD	5257.2	-569
196	NVDD	5337.2	-569
197	NVDD	5417.2	-569
198	NVDD	5497.2	-569
199	NVDD	5577.2	-569
200	NVDD	5657.2	-569
201	NVDD	5737.2	-569
202	CD2N	5817.2	-569

PAD	NAME	X	Y
203	CD2N	5897.2	-569
204	CD2N	5977.2	-569
205	CD2N	6057.2	-569
206	CD2P	6137.2	-569
207	CD2P	6217.2	-569
208	CD2P	6297.2	-569
209	CD2P	6377.2	-569
210	MV3	6457.2	-569
211	MV3	6537.2	-569
212	MV3	6617.2	-569
213	MV3	6697.2	-569
214	MV3	6777.2	-569
215	MV3	6857.2	-569
216	MV3	6937.2	-569
217	MV3S	7017.2	-569
218	CB1N	7097.2	-569
219	CB1N	7177.2	-569
220	CB1N	7257.2	-569
221	CB1N	7337.2	-569
222	CB1P	7417.2	-569
223	CB1P	7497.2	-569
224	CB1P	7577.2	-569
225	CB1P	7657.2	-569
226	V3I	7737.2	-569
227	V3I	7817.2	-569
228	V3I	7897.2	-569
229	V3I	7977.2	-569
230	V3S	8057.2	-569
231	V3O	8137.2	-569
232	V3O	8217.2	-569
233	V3O	8297.2	-569
234	CE1P	8377.2	-569
235	CE1P	8457.2	-569
236	CE1N	8537.2	-569
237	CE1N	8617.2	-569

PAD	NAME	X	Y
238	CE3P	8697.2	-569
239	CE3P	8777.2	-569
240	CE2N	8857.2	-569
241	CE2N	8937.2	-569
242	CE2P	9017.2	-569
243	CE2P	9097.2	-569
244	VOUT	9177.2	-569
245	VOUT	9257.2	-569
246	VOUT	9337.2	-569
247	VOUT	9417.2	-569
248	VOUT	9497.2	-569
249	Reserved	9645.4	-550.3
250	Reserved	9834.6	-528.7
251	COM4	10287	-540
252	COM5	10287	-495
253	COM6	10287	-450
254	COM7	10287	-405
255	COM12	10287	-360
256	COM13	10287	-315
257	COM14	10287	-270
258	COM15	10287	-225
259	COM20	10287	-180
260	COM21	10287	-135
261	COM22	10287	-90
262	COM23	10287	-45
263	COM28	10287	0
264	COM29	10287	45
265	COM30	10287	90
266	COM31	10287	135
267	COM36	10287	180
268	COM37	10287	225
269	COM38	10287	270
270	COM39	10287	315
271	COM44	10287	360
272	COM45	10287	405

PAD	NAME	X	Y
273	COM46	10287	450
274	COM47	10287	495
275	COM52	10287	540
276	COM53	9826.8	547
277	COM54	9781.8	547
278	COM55	9736.8	547
279	COM60	9691.8	547
280	COM61	9646.8	547
281	COM62	9601.8	547
282	COM63	9556.8	547
283	COM68	9511.8	547
284	COM69	9466.8	547
285	COM70	9421.8	547
286	COM71	9376.8	547
287	COM76	9331.8	547
288	COM77	9286.8	547
289	COM78	9241.8	547
290	COM79	9196.8	547
291	COM84	9151.8	547
292	COM85	9106.8	547
293	COM86	9061.8	547
294	COM87	9016.8	547
295	COM92	8971.8	547
296	COM93	8926.8	547
297	COM94	8881.8	547
298	COM95	8836.8	547
299	COM100	8791.8	547
300	COM101	8746.8	547
301	COM102	8701.8	547
302	COM103	8656.8	547
303	COM108	8611.8	547
304	COM109	8566.8	547
305	COM110	8521.8	547
306	COM111	8476.8	547
307	COM116	8431.8	547

PAD	NAME	X	Y
308	COM117	8386.8	547
309	COM118	8341.8	547
310	COM119	8296.8	547
311	COM124	8251.8	547
312	COM125	8206.8	547
313	COM126	8161.8	547
314	COM127	8116.8	547
315	COM132	8071.8	547
316	COM133	8026.8	547
317	COM134	7981.8	547
318	COM135	7936.8	547
319	COM140	7891.8	547
320	COM141	7846.8	547
321	COM142	7801.8	547
322	COM143	7756.8	547
323	COM148	7711.8	547
324	COM149	7666.8	547
325	COM150	7621.8	547
326	COM151	7576.8	547
327	COM156	7531.8	547
328	COM157	7486.8	547
329	COM158	7441.8	547
330	COM159	7396.8	547
331	COM164	7351.8	547
332	COM165	7306.8	547
333	COM166	7261.8	547
334	COM167	7216.8	547
335	COM172	7171.8	547
336	COM173	7126.8	547
337	COM174	7081.8	547
338	COM175	7036.8	547
339	COM180	6991.8	547
340	COM181	6946.8	547
341	COM182	6901.8	547
342	COM183	6856.8	547

PAD	NAME	X	Y
343	COM188	6811.8	547
344	COM189	6766.8	547
345	COM190	6721.8	547
346	COM191	6676.8	547
347	COM196	6631.8	547
348	COM197	6586.8	547
349	COM198	6541.8	547
350	COM199	6496.8	547
351	COM204	6451.8	547
352	COM205	6406.8	547
353	COM206	6361.8	547
354	COM207	6316.8	547
355	COM212	6271.8	547
356	COM213	6226.8	547
357	COM214	6181.8	547
358	COM215	6136.8	547
359	COM220	6091.8	547
360	COM221	6046.8	547
361	COM222	6001.8	547
362	COM223	5956.8	547
363	COM228	5911.8	547
364	COM229	5866.8	547
365	COM230	5821.8	547
366	COM231	5776.8	547
367	COM236	5731.8	547
368	COM237	5686.8	547
369	COM238	5641.8	547
370	COM239	5596.8	547
371	SEG319	5423	547
372	SEG318	5389	547
373	SEG317	5355	547
374	SEG316	5321	547
375	SEG315	5287	547
376	SEG314	5253	547
377	SEG313	5219	547

PAD	NAME	X	Y
378	SEG312	5185	547
379	SEG311	5151	547
380	SEG310	5117	547
381	SEG309	5083	547
382	SEG308	5049	547
383	SEG307	5015	547
384	SEG306	4981	547
385	SEG305	4947	547
386	SEG304	4913	547
387	SEG303	4879	547
388	SEG302	4845	547
389	SEG301	4811	547
390	SEG300	4777	547
391	SEG299	4743	547
392	SEG298	4709	547
393	SEG297	4675	547
394	SEG296	4641	547
395	SEG295	4607	547
396	SEG294	4573	547
397	SEG293	4539	547
398	SEG292	4505	547
399	SEG291	4471	547
400	SEG290	4437	547
401	SEG289	4403	547
402	SEG288	4369	547
403	SEG287	4335	547
404	SEG286	4301	547
405	SEG285	4267	547
406	SEG284	4233	547
407	SEG283	4199	547
408	SEG282	4165	547
409	SEG281	4131	547
410	SEG280	4097	547
411	SEG279	4063	547
412	SEG278	4029	547

PAD	NAME	X	Y
413	SEG277	3995	547
414	SEG276	3961	547
415	SEG275	3927	547
416	SEG274	3893	547
417	SEG273	3859	547
418	SEG272	3825	547
419	SEG271	3791	547
420	SEG270	3757	547
421	SEG269	3723	547
422	SEG268	3689	547
423	SEG267	3655	547
424	SEG266	3621	547
425	SEG265	3587	547
426	SEG264	3553	547
427	SEG263	3519	547
428	SEG262	3485	547
429	SEG261	3451	547
430	SEG260	3417	547
431	SEG259	3383	547
432	SEG258	3349	547
433	SEG257	3315	547
434	SEG256	3281	547
435	SEG255	3247	547
436	SEG254	3213	547
437	SEG253	3179	547
438	SEG252	3145	547
439	SEG251	3111	547
440	SEG250	3077	547
441	SEG249	3043	547
442	SEG248	3009	547
443	SEG247	2975	547
444	SEG246	2941	547
445	SEG245	2907	547
446	SEG244	2873	547
447	SEG243	2839	547

PAD	NAME	X	Y
448	SEG242	2805	547
449	SEG241	2771	547
450	SEG240	2737	547
451	SEG239	2703	547
452	SEG238	2669	547
453	SEG237	2635	547
454	SEG236	2601	547
455	SEG235	2567	547
456	SEG234	2533	547
457	SEG233	2499	547
458	SEG232	2465	547
459	SEG231	2431	547
460	SEG230	2397	547
461	SEG229	2363	547
462	SEG228	2329	547
463	SEG227	2295	547
464	SEG226	2261	547
465	SEG225	2227	547
466	SEG224	2193	547
467	SEG223	2159	547
468	SEG222	2125	547
469	SEG221	2091	547
470	SEG220	2057	547
471	SEG219	2023	547
472	SEG218	1989	547
473	SEG217	1955	547
474	SEG216	1921	547
475	SEG215	1887	547
476	SEG214	1853	547
477	SEG213	1819	547
478	SEG212	1785	547
479	SEG211	1751	547
480	SEG210	1717	547
481	SEG209	1683	547
482	SEG208	1649	547

PAD	NAME	X	Y
483	SEG207	1615	547
484	SEG206	1581	547
485	SEG205	1547	547
486	SEG204	1513	547
487	SEG203	1479	547
488	SEG202	1445	547
489	SEG201	1411	547
490	SEG200	1377	547
491	SEG199	1343	547
492	SEG198	1309	547
493	SEG197	1275	547
494	SEG196	1241	547
495	SEG195	1207	547
496	SEG194	1173	547
497	SEG193	1139	547
498	SEG192	1105	547
499	SEG191	1071	547
500	SEG190	1037	547
501	SEG189	1003	547
502	SEG188	969	547
503	SEG187	935	547
504	SEG186	901	547
505	SEG185	867	547
506	SEG184	833	547
507	SEG183	799	547
508	SEG182	765	547
509	SEG181	731	547
510	SEG180	697	547
511	SEG179	663	547
512	SEG178	629	547
513	SEG177	595	547
514	SEG176	561	547
515	SEG175	527	547
516	SEG174	493	547
517	SEG173	459	547

PAD	NAME	X	Y
518	SEG172	425	547
519	SEG171	391	547
520	SEG170	357	547
521	SEG169	323	547
522	SEG168	289	547
523	SEG167	255	547
524	SEG166	221	547
525	SEG165	187	547
526	SEG164	153	547
527	SEG163	119	547
528	SEG162	85	547
529	SEG161	51	547
530	SEG160	17	547
531	SEG159	-17	547
532	SEG158	-51	547
533	SEG157	-85	547
534	SEG156	-119	547
535	SEG155	-153	547
536	SEG154	-187	547
537	SEG153	-221	547
538	SEG152	-255	547
539	SEG151	-289	547
540	SEG150	-323	547
541	SEG149	-357	547
542	SEG148	-391	547
543	SEG147	-425	547
544	SEG146	-459	547
545	SEG145	-493	547
546	SEG144	-527	547
547	SEG143	-561	547
548	SEG142	-595	547
549	SEG141	-629	547
550	SEG140	-663	547
551	SEG139	-697	547
552	SEG138	-731	547

PAD	NAME	X	Y
553	SEG137	-765	547
554	SEG136	-799	547
555	SEG135	-833	547
556	SEG134	-867	547
557	SEG133	-901	547
558	SEG132	-935	547
559	SEG131	-969	547
560	SEG130	-1003	547
561	SEG129	-1037	547
562	SEG128	-1071	547
563	SEG127	-1105	547
564	SEG126	-1139	547
565	SEG125	-1173	547
566	SEG124	-1207	547
567	SEG123	-1241	547
568	SEG122	-1275	547
569	SEG121	-1309	547
570	SEG120	-1343	547
571	SEG119	-1377	547
572	SEG118	-1411	547
573	SEG117	-1445	547
574	SEG116	-1479	547
575	SEG115	-1513	547
576	SEG114	-1547	547
577	SEG113	-1581	547
578	SEG112	-1615	547
579	SEG111	-1649	547
580	SEG110	-1683	547
581	SEG109	-1717	547
582	SEG108	-1751	547
583	SEG107	-1785	547
584	SEG106	-1819	547
585	SEG105	-1853	547
586	SEG104	-1887	547
587	SEG103	-1921	547

PAD	NAME	X	Y
588	SEG102	-1955	547
589	SEG101	-1989	547
590	SEG100	-2023	547
591	SEG99	-2057	547
592	SEG98	-2091	547
593	SEG97	-2125	547
594	SEG96	-2159	547
595	SEG95	-2193	547
596	SEG94	-2227	547
597	SEG93	-2261	547
598	SEG92	-2295	547
599	SEG91	-2329	547
600	SEG90	-2363	547
601	SEG89	-2397	547
602	SEG88	-2431	547
603	SEG87	-2465	547
604	SEG86	-2499	547
605	SEG85	-2533	547
606	SEG84	-2567	547
607	SEG83	-2601	547
608	SEG82	-2635	547
609	SEG81	-2669	547
610	SEG80	-2703	547
611	SEG79	-2737	547
612	SEG78	-2771	547
613	SEG77	-2805	547
614	SEG76	-2839	547
615	SEG75	-2873	547
616	SEG74	-2907	547
617	SEG73	-2941	547
618	SEG72	-2975	547
619	SEG71	-3009	547
620	SEG70	-3043	547
621	SEG69	-3077	547
622	SEG68	-3111	547

PAD	NAME	X	Y
623	SEG67	-3145	547
624	SEG66	-3179	547
625	SEG65	-3213	547
626	SEG64	-3247	547
627	SEG63	-3281	547
628	SEG62	-3315	547
629	SEG61	-3349	547
630	SEG60	-3383	547
631	SEG59	-3417	547
632	SEG58	-3451	547
633	SEG57	-3485	547
634	SEG56	-3519	547
635	SEG55	-3553	547
636	SEG54	-3587	547
637	SEG53	-3621	547
638	SEG52	-3655	547
639	SEG51	-3689	547
640	SEG50	-3723	547
641	SEG49	-3757	547
642	SEG48	-3791	547
643	SEG47	-3825	547
644	SEG46	-3859	547
645	SEG45	-3893	547
646	SEG44	-3927	547
647	SEG43	-3961	547
648	SEG42	-3995	547
649	SEG41	-4029	547
650	SEG40	-4063	547
651	SEG39	-4097	547
652	SEG38	-4131	547
653	SEG37	-4165	547
654	SEG36	-4199	547
655	SEG35	-4233	547
656	SEG34	-4267	547
657	SEG33	-4301	547

PAD	NAME	X	Y
658	SEG32	-4335	547
659	SEG31	-4369	547
660	SEG30	-4403	547
661	SEG29	-4437	547
662	SEG28	-4471	547
663	SEG27	-4505	547
664	SEG26	-4539	547
665	SEG25	-4573	547
666	SEG24	-4607	547
667	SEG23	-4641	547
668	SEG22	-4675	547
669	SEG21	-4709	547
670	SEG20	-4743	547
671	SEG19	-4777	547
672	SEG18	-4811	547
673	SEG17	-4845	547
674	SEG16	-4879	547
675	SEG15	-4913	547
676	SEG14	-4947	547
677	SEG13	-4981	547
678	SEG12	-5015	547
679	SEG11	-5049	547
680	SEG10	-5083	547
681	SEG9	-5117	547
682	SEG8	-5151	547
683	SEG7	-5185	547
684	SEG6	-5219	547
685	SEG5	-5253	547
686	SEG4	-5287	547
687	SEG3	-5321	547
688	SEG2	-5355	547
689	SEG1	-5389	547
690	SEG0	-5423	547
691	COM235	-5596.8	547
692	COM234	-5641.8	547

PAD	NAME	X	Y
693	COM233	-5686.8	547
694	COM232	-5731.8	547
695	COM227	-5776.8	547
696	COM226	-5821.8	547
697	COM225	-5866.8	547
698	COM224	-5911.8	547
699	COM219	-5956.8	547
700	COM218	-6001.8	547
701	COM217	-6046.8	547
702	COM216	-6091.8	547
703	COM211	-6136.8	547
704	COM210	-6181.8	547
705	COM209	-6226.8	547
706	COM208	-6271.8	547
707	COM203	-6316.8	547
708	COM202	-6361.8	547
709	COM201	-6406.8	547
710	COM200	-6451.8	547
711	COM195	-6496.8	547
712	COM194	-6541.8	547
713	COM193	-6586.8	547
714	COM192	-6631.8	547
715	COM187	-6676.8	547
716	COM186	-6721.8	547
717	COM185	-6766.8	547
718	COM184	-6811.8	547
719	COM179	-6856.8	547
720	COM178	-6901.8	547
721	COM177	-6946.8	547
722	COM176	-6991.8	547
723	COM171	-7036.8	547
724	COM170	-7081.8	547
725	COM169	-7126.8	547
726	COM168	-7171.8	547
727	COM163	-7216.8	547

PAD	NAME	X	Y
728	COM162	-7261.8	547
729	COM161	-7306.8	547
730	COM160	-7351.8	547
731	COM155	-7396.8	547
732	COM154	-7441.8	547
733	COM153	-7486.8	547
734	COM152	-7531.8	547
735	COM147	-7576.8	547
736	COM146	-7621.8	547
737	COM145	-7666.8	547
738	COM144	-7711.8	547
739	COM139	-7756.8	547
740	COM138	-7801.8	547
741	COM137	-7846.8	547
742	COM136	-7891.8	547
743	COM131	-7936.8	547
744	COM130	-7981.8	547
745	COM129	-8026.8	547
746	COM128	-8071.8	547
747	COM123	-8116.8	547
748	COM122	-8161.8	547
749	COM121	-8206.8	547
750	COM120	-8251.8	547
751	COM115	-8296.8	547
752	COM114	-8341.8	547
753	COM113	-8386.8	547
754	COM112	-8431.8	547
755	COM107	-8476.8	547
756	COM106	-8521.8	547
757	COM105	-8566.8	547
758	COM104	-8611.8	547
759	COM99	-8656.8	547
760	COM98	-8701.8	547
761	COM97	-8746.8	547
762	COM96	-8791.8	547

PAD	NAME	X	Y
763	COM91	-8836.8	547
764	COM90	-8881.8	547
765	COM89	-8926.8	547
766	COM88	-8971.8	547
767	COM83	-9016.8	547
768	COM82	-9061.8	547
769	COM81	-9106.8	547
770	COM80	-9151.8	547
771	COM75	-9196.8	547
772	COM74	-9241.8	547
773	COM73	-9286.8	547
774	COM72	-9331.8	547
775	COM67	-9376.8	547
776	COM66	-9421.8	547
777	COM65	-9466.8	547
778	COM64	-9511.8	547
779	COM59	-9556.8	547
780	COM58	-9601.8	547
781	COM57	-9646.8	547
782	COM56	-9691.8	547
783	COM51	-9736.8	547
784	COM50	-9781.8	547
785	COM49	-9826.8	547

Unit : um

5 BLOCK DIAGRAM

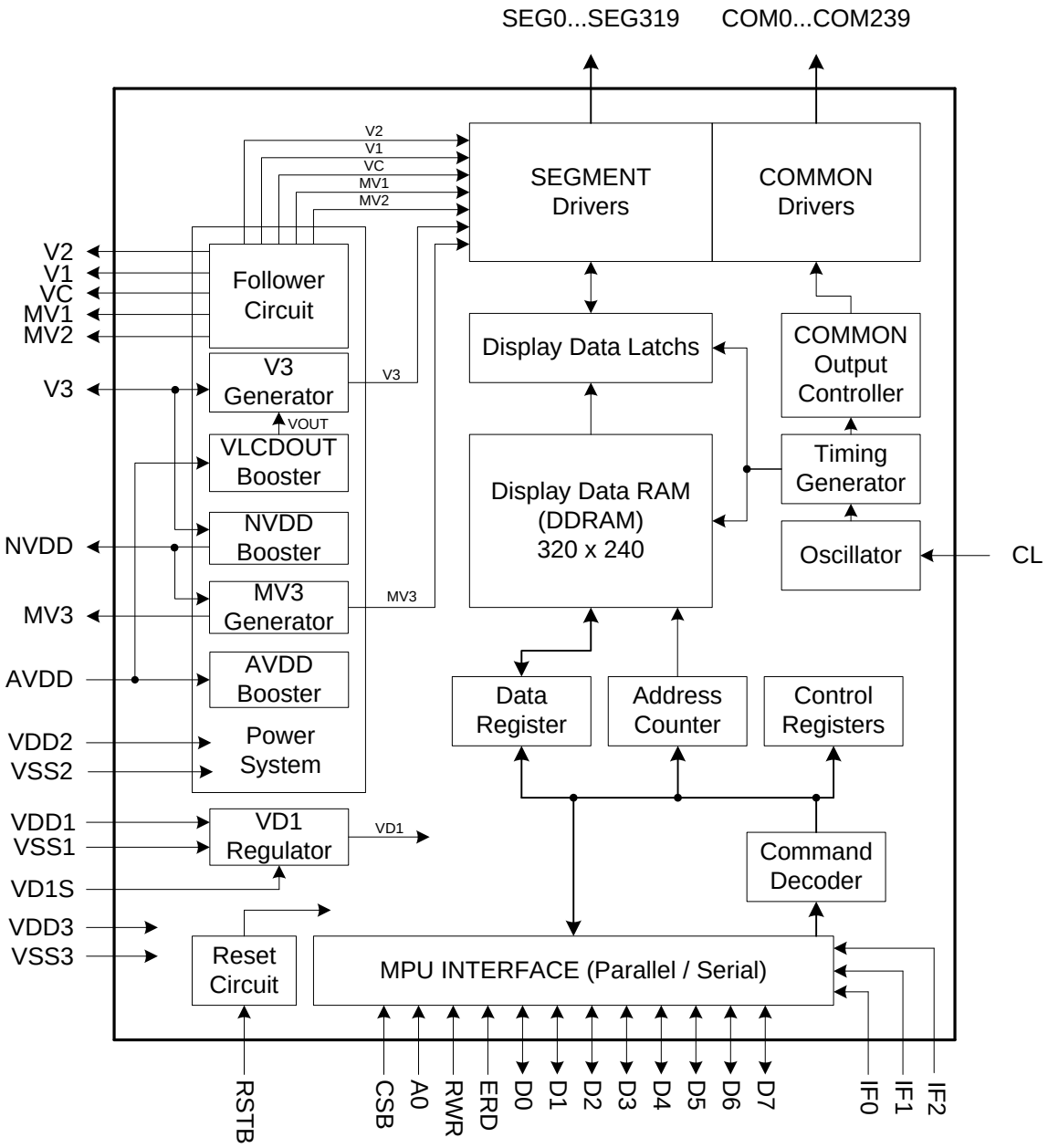


Figure 2 Block Diagram

6 PIN DESCRIPTION

6.1 Power System

Name	Type	Description
VDD1	Power	VDD1 is the power of interface I/O circuit and OSC circuit.
VDD2	Power	VDD2 is the analog power for booster circuit and OP. VDD2 and VDD3 are connected together
VDD3	Power	VDD3 is the power of VREF circuit.
VSS1	Power	Ground of interface, logic and OSC circuit. Ground system should be connected together.
VSS2	Power	Ground of booster circuit and OP. Ground system should be connected together.
VSS3	Power	Ground of VREF circuit. Ground system should be connected together.

6.2 LCD Driver Supply

Name	Type	Description
VOUT	Power	VOUT is the source of V3 regulator.
AVDD	Power	DC/DC converter for LCD driver circuit.
NVDD	Power	DC/DC converter for LCD driver circuit.
V3O V3I V3S	Power	LCD driver supply. V3O is the output voltage of V3 generator. V3I is the V3 supply of LCD drivers. V3S is the sensor of the V3 generator. V3O, V3I and V3S should be connected together.
V2	Power	LCD driver supply.
V1	Power	LCD driver supply.
VC	Power	LCD driver supply for center level. VC should be connected with ground system.
MV1	Power	LCD driver supply.
MV2	Power	LCD driver supply.
MV3 MV3S	Power	LCD driver supply. MV3 is the output voltage of MV3 generator. MV3S is the sensor of the MV3 generator. MV3 and MV3S should be connected together.
CA1P CA1N CA2P CA2N	Power	Positive output of AVDD power. Connects a non-polar capacitor between CA1P and CA1N. Connects a non-polar capacitor between CA2P and CA2N.
CB1P CB1N	Power	Negative output of MV3 power. Connects a non-polar capacitor between CB1P pin and CB1N pin.
CD1P CD1N CD2P CD2N	Power	Negative output NVDD power. Connects a non-polar capacitor between CD1P pin and CD1N pin. Connects a non-polar capacitor between CD2P pin and CD2N pin.

Name	Type	Description
CE1P CE1N CE2P CE2N CE3P	Power	Positive output of VOUT power. Connects a non-polar capacitor between CE1P and CE1N. Connects a non-polar capacitor between CE2P and CE2N. Connects a non-polar capacitor between CE3P and CE1N.

6.3 System Control

Name	Type	Description
VD1S	I	This pin is used to set VD1 generation circuit ON or OFF. VD1S = "L": VD1 generation circuit is disabled. VD1S = "H": VD1 generation circuit is enabled. **VDD1** / **Level of VD1S** 2.7V~3.6V / L (VSS1) 4.5V~5.5V / H (VDD1)
VD1I VD1O	I/O	VD1I is the power supply pin of the internal digital circuits. VD1O is the VD1 output. VD1I and VD1O should be connected together.
CLS	I	When using internal clock oscillator, please connect this pin to "H" by VDD1. When using external clock oscillator, please connect this pin to "L" by VSS1.
CL	I/O	When using internal clock oscillator, this pin must be floating. When using external clock oscillator, this pin is oscillator input.
VPP	I	The programming power supply of the built-in OTP. Apply external power VPP = 6.5V when programming.
EXTB	I	EXTB="L": Enable the extension operation mode. When programming OTP, connect EXTB to VSS1 externally. This pin has an internal pull-high resistor. Please leave this pin floating after extension operation mode.

6.4 LCD Driver Outputs

Name	Type	Description
SEG0 to SEG319	O	LCD SEG-driver outputs. One voltage level of V2, V1, VC, MV1 and MV2 is selected by combining display DDRAM.
COM0 to COM239	O	LCD COM-driver outputs. One voltage level of V3, VC and MV3 is selected by combining display DDRAM.

6.5 Microprocessor Interface

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin. When RSTB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>IF[2:0]</td><td>I</td><td>These pins select interface operation mode.
<table>
<tr><th>IF2</th><th>IF1</th><th>IF0</th><th>MCU interface type</th></tr>
<tr><td>L</td><td>H</td><td>H</td><td>80 series 8-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>8-bit serial (4-Line)</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>9-bit serial (3-Line)</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>I2C interface</td></tr>
</table>
Note: Refer to “Parallel / Serial Interface” for detailed information.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin.
CSB=“L”: This chip is selected and the MCU interface is active.
CSB=“H”: This chip is not selected and the MCU interface is disabled (D[7:0] are high impedance).
CSB is not used in I2C interface. Please fix to “H” by VDD1.</td></tr>
<tr><td>A0</td><td>I</td><td>A0 determines whether the access is related data or command.
In parallel interface and 4-Line SPI: A0 is register selection input.
A0 = "H": inputs on data bus are display data;
A0 = "L": inputs on data bus are command.
A0 is not used in 3-Line SPI and I2C interface. Please fix to “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>I</td><td>Read / Write execution control pin.
<table>
<tr><th>MCU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
R/W = “H” : read
R/W = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin.
The data are latched at the rising edge of the /WR signal.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to “H” by VDD1.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>ERD</td><td>I</td><td>Read / Write execution control pin.
<table>
<tr><th>MCU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin.
R/W = “H”: When E is “H”, data bus is in output status.
R/W = “L”: The data are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, data bus is in output status.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to “H” by VDD1.</td></tr>
<tr><td>D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: 6800 or 8080 mode
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
Note : When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.

When using serial interface: 3 Line SPI , 4 Line SPI
D[0] : serial input clock (SCL).
D[1] : serial input clock (SDA_IN).
D[2:3] : serial output data (SDA_OUT).
D[4:7] : fix to “H” by VDD1.
D[1:3] must be connected together for SDA.

When using I2C interface:
D[0]: serial clock input (SCL)
D[1]: serial data input (SDA_IN).
D[5:2]: serial data output (SDA_OUT).
D[7:6]: slave addresses (SA1~SA0) and must be fixed to “H” or “L”.
D[1:5] must be connected together for SDA.

The ITO resistance on SDA/SCL will form a voltage divider with the pull-up resistor on system. To keep the signal quality better, customers should keep the ITO resistance as low as possible.</td></tr>
</table>

6.6 Test Pins

Name	Type	Description
TCAP	Test	Reserved for testing only. Leave this pin open.
VREF	Test	Reserved for testing only. Leave this pin open.
T0~T17	Test	Reserved for testing only. Leave those pins open.
TF[1:0]	Test	Reserved for testing only. Leave those pins open.

6.7 ITO Resistance Limitation

Pin Name	ITO Resister
VPP, VDD1, VDD2, VDD3, VSS1, VSS2, VSS3	<50Ω
VD1I, VD1O, V3O, V3I, V3S, V2, V1, VC, MV1, MV2, MV3, MV3S, AVDD, NVDD, CA1P, CA1N, CA2P, CA2N, CB1P, CB1N, CD1P, CD1N, CD2P, CD2N, CE1P , CE1N, CE2P, CE2N, CE3P, VOUT	<100Ω
SCL(I2C), SDA(I2C)	<100Ω
A0, ERD, RWR, CSB, D[7:0],VD1S	<700Ω
IF[2:0], CLS, EXTB	<1KΩ
RSTB	<5KΩ *4
TCAP, CL, VREF, T0~T17, TF0, TF1	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM239 is equal, and so is it of SEG0 ~ SEG319.
2. These limitations include the bottleneck of ITO layout.
3. The ITO impedance suggestions are listed above.
4. The resistance of RSTB is 2KΩ~5KΩ generally. It can be the combination of ITO and external resistor.

6.8 ITO Layout Guide

The ITO layout suggestion is shown as below:

- **For V3, MV3, VDD, VSS and VD1**

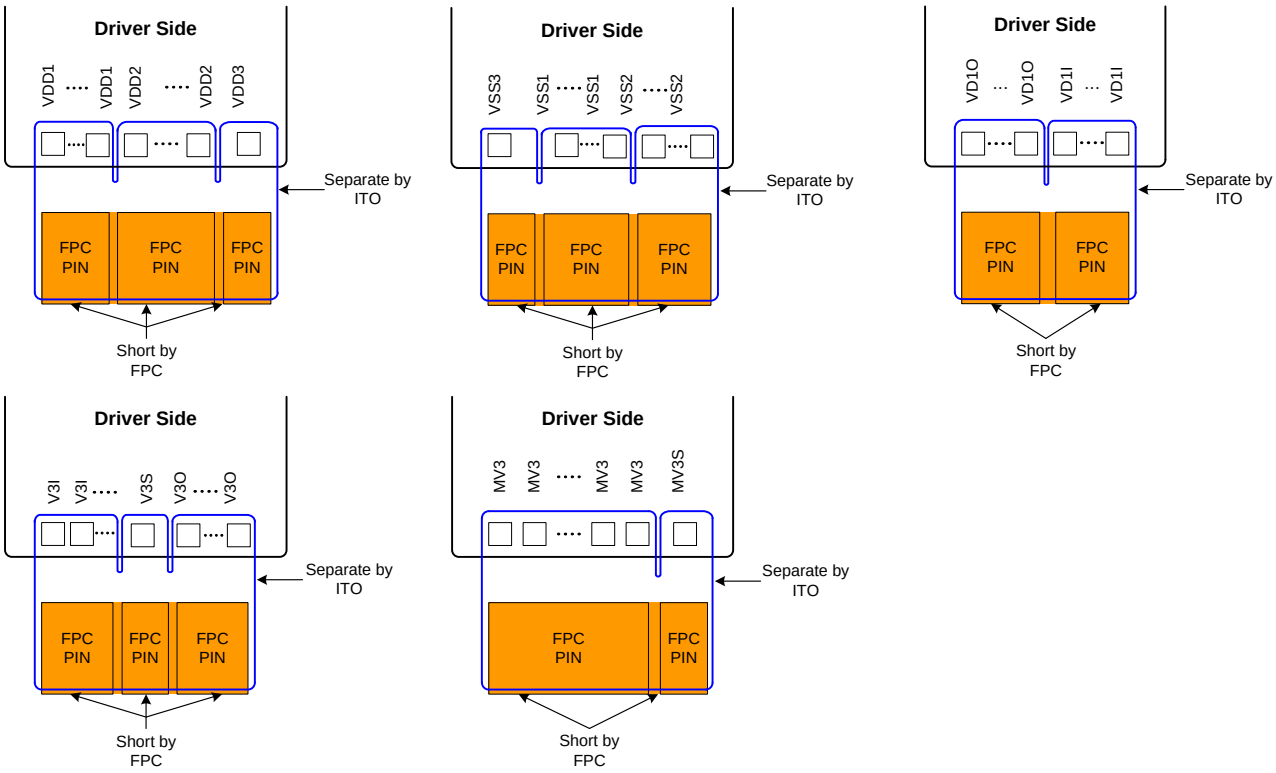


Figure 3 Power Pin ITO Layout

6.9 For VPP

This is the power source for programming the internal OTP. If the ITO resistance is too high, the operation current will cause the voltage drop while programming OTP. Please try to keep the ITO resistance as low as possible.

6.10 Enhance ESD performance for COG application

1. Increase RSTB resistance:

Figure 4 RSTB ITO Layout

2. Add ESD protection ring:

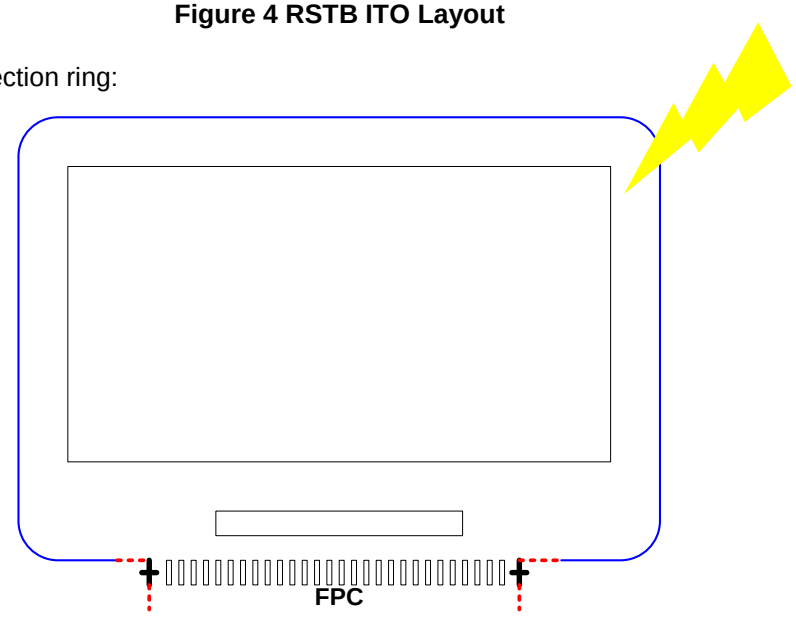


Figure 5 Air ESD Protection Ring

Note: Please short the ESD protection ring to VSS of external device.

7 FUNCTION DESCRIPTION

7.1 Microprocessor Interface

7.1.1 Chip Select Input

CSB pin is used for chip selection. ST75320 can interface with a MCU when CSB is “L”. If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interfaces, the internal shift register and serial counter are reset when CSB is “H”.

7.1.2 Parallel / Serial Interface

The ST75320 has types of interface for kinds of MPU. The MPU interface selection is selected by IF[2:0] pins as shown in Table 1.

Table 1 Parallel/Serial Interface Mode

Setting			MCU Type	Interface Pin Function				
IF2	IF1	IF0		CSB	A0	RWR	ERD	D[7:0]
L	H	H	Parallel 8080	CSB	A0	/WR	/RD	D[7:0]
L	H	L	Parallel 6800			R/W	E	
L	L	H	Serial 4-Line			--	--	Refer to serial interface.
L	L	L	Serial 3-Line		--	--	--	
H	H	L	Serial I2C	--	--	--	--	Refer to serial interface.

7.1.3 Parallel Interface

When IF2 = “L” and IF1 =”H”, the 8-bit bi-directional parallel interface is enabled, and the type of MPU is selected by “IF0” pin. The type of data transfer is determined by signals at A0, ERD, and RWR as shown in Table2.

Table 2 Microprocessor Selection for Parallel Interface

Common Pins		6800-Series		8080-Series		Description
CSB	A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
“L”	H	H	H	L	H	Display data read out
	H	H	L	H	L	Display data write
	L	H	H	L	H	Internal status read
	L	H	L	H	L	Writes to internal register (instruction)

7.1.4 Serial Interface

The setting IF[2:0], one of the Serial Interfaces can be selected.

Interface	IF[2:0]	CSB	A0	ERD	RWR	D[7:0]
4-Line SPI	L, L, H	CSB	A0	---	---	D[0]= SCL , D[1]=SDA_IN, D[2:3]= SDA_OUT, D[4:7] = --
3-Line SPI	L, L, L	CSB	---	---	---	
I^2C interface	H, H, L	---	---	---	---	D[0] : SCL, D[1] : SDA_IN, D[5:2] : SDA_OUT, D[7:6] : SA[1:0], I2C slave address bit..

Note : The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

.4-Line Serial Interface

When CSB is active (CSB=“L”), serial data (SDA) and serial clock (SCLK) inputs are enabled. When CSB is not active (CSB=“H”), the internal shift register and counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCL. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is “H” and will be instruction when A0 is “L”. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCL signal quality is very important and external noise maybe causes unexpected

data/instruction latch.

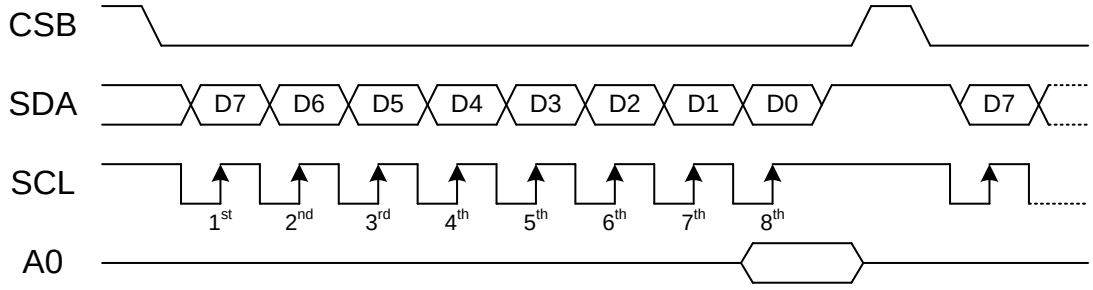
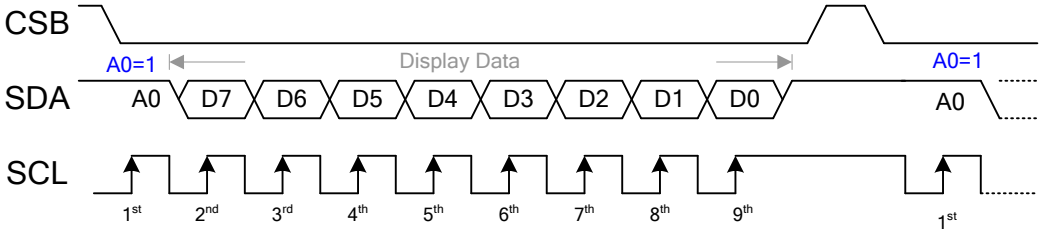


Figure 6 Write-Operation of 4-Line Serial Interface

7.1.6 3-Line serial Interface

The 3-Line SPI (9-bit) uses 3 pins (CSB, SDA & SCL) to communicate with MPU. When CSB is "L", IC is active and the SDA and SCL pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9th) clock. After CSB returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit at the 1st bit of each 9-bit serial data.

When A0 is "1", the transferred 8-bit is parameter.



When A0 is "0", the transferred 8-bit is instruction.

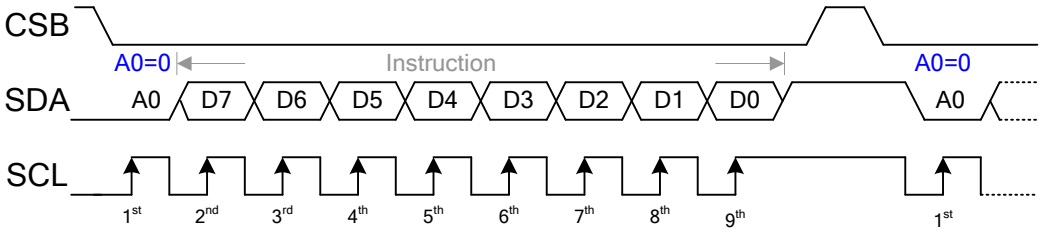


Figure 7 Write-Operation of 3-Line Serial Interface

7.1.7 I²C Interface

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in **Figure 8**.

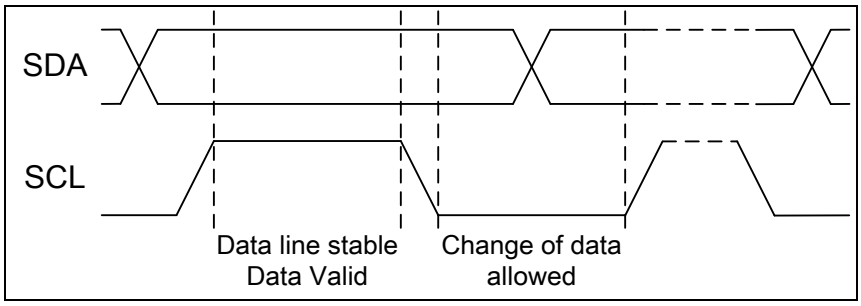


Figure 8 Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in **Figure 9**.

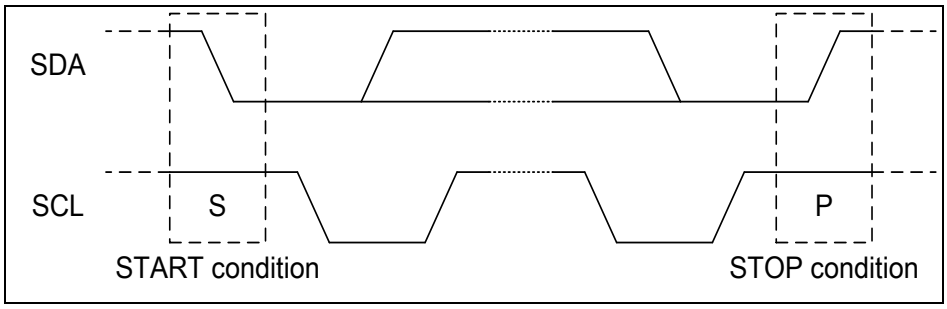


Figure 9 Definition of START and STOP Condition

SYSTEM CONFIGURATION

The system configuration is illustrated in **Figure 10** and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

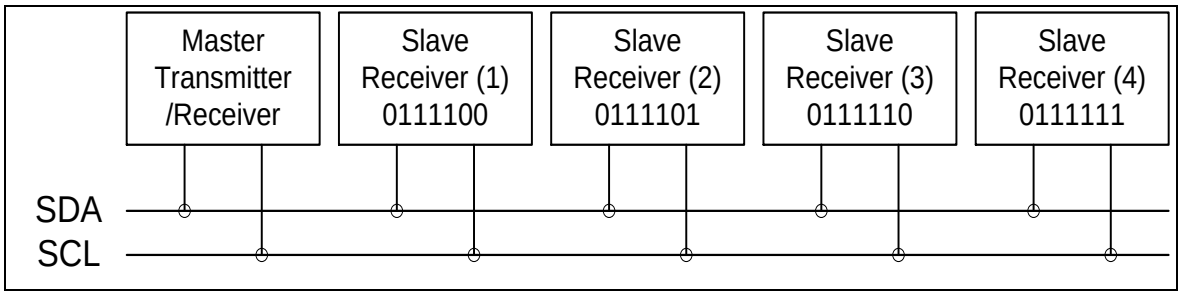


Figure 10 System Configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated in **Figure 11**.

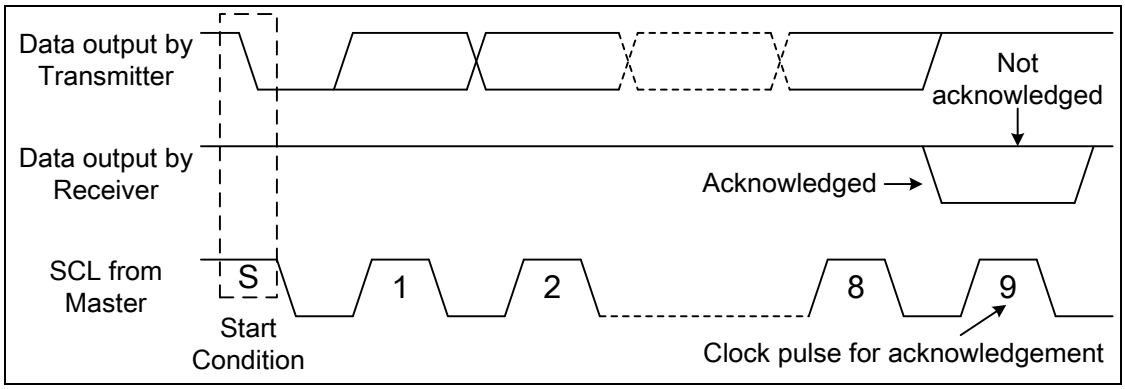


Figure 11 Acknowledgement of I^2C Interface

I²C INTERFACE PROTOCOL

ST75320 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (01111**00**, 01111**01**, 01111**10** and 01111**11**) are reserved for ST75320. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1).The I²C Interface protocol is illustrated in **Figure 12**.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address and A0. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST75320 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST75320 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

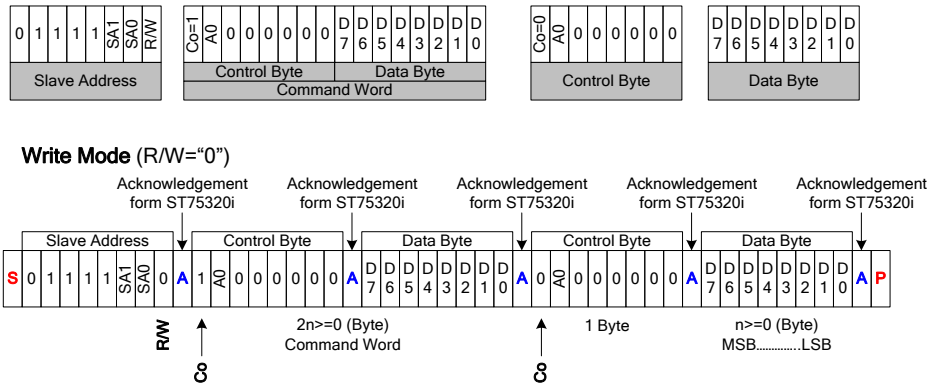


Figure 12 I²C Interface Protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

7.2 Display Data RAM (DDRAM)

ST75320 containing a 320x240 bits static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 320 columns by 240 rows. When the data bit in DDRAM is “1”, the segment driver will output “ON” voltage. If it is “0”, the segment driver will output “OFF” voltage. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.

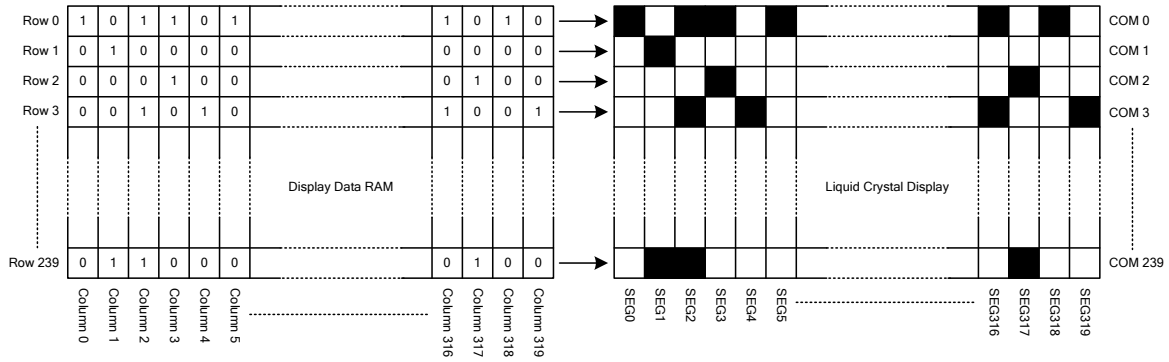


Figure 13 DDRAM Mapping

7.2.1 Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates a 6-bit Page Address Register which can be modified by the instruction of Page Address Set only. As shown in **Figure 14**, the 240 rows are configured as 30 pages with 8-bit. The page address must be set before accessing DDRAM content.

7.2.2 Column Address Circuit

This circuit provides the column address of DDRAM. It incorporates a 9-bit Column Address Register which can be modified by the instruction of “Column Address” only. The column address must be set before accessing DDRAM content.

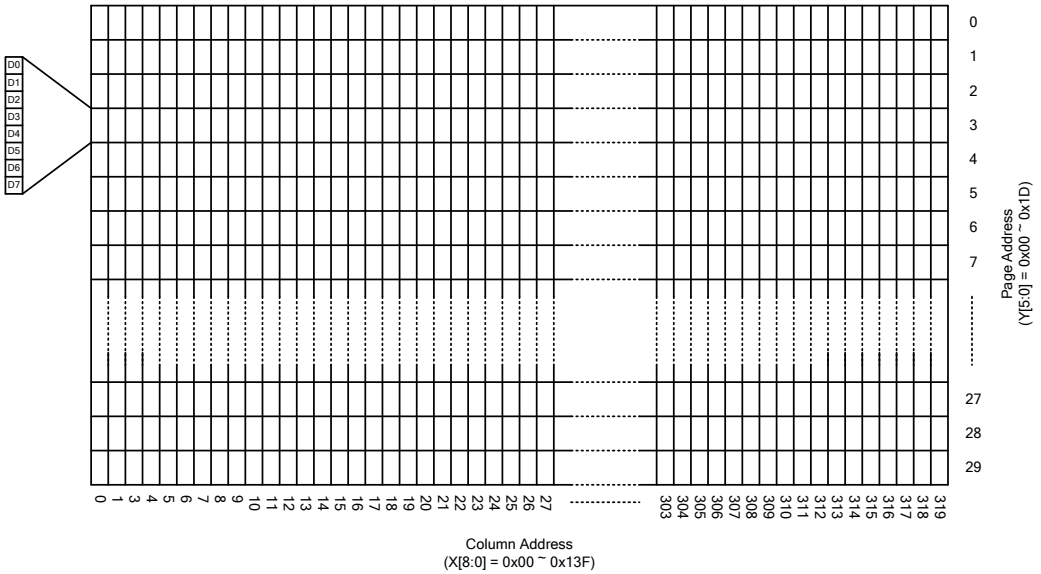


Figure 14 DDRAM Format

7.3 LCD Display Function

7.3.1 DDRAM Map to LCD Driver Output

The relation between DDRAM and outputs with different MX or MY setting is shown below.

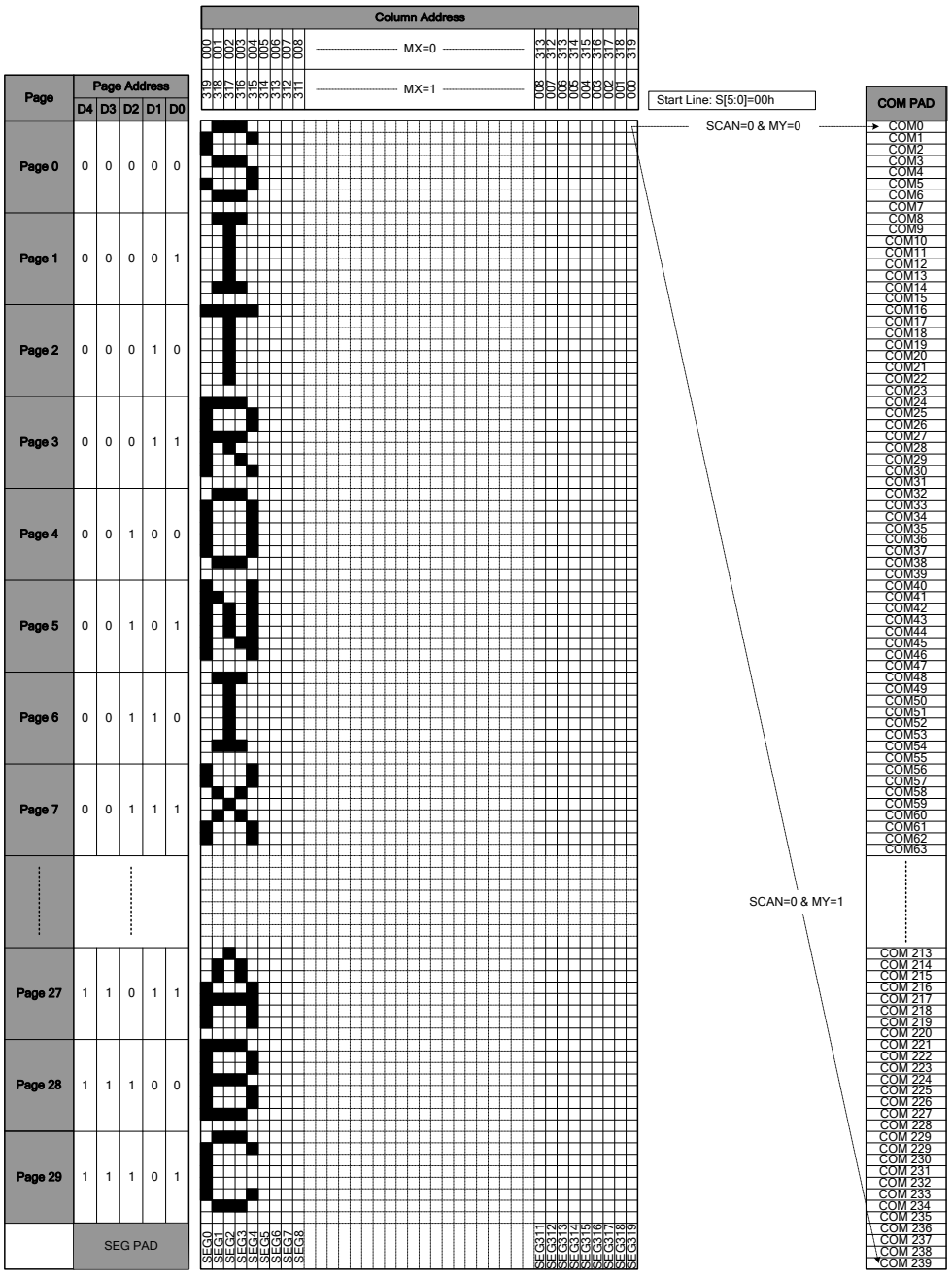


Figure 15 DDRAM Display Direction (Normal Scan)

7.3.2 Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (setting by instruction of Display Area Set) of the display. Therefore, by setting Line Address repeatedly, ST75320 is possible to realize the screen scrolling (4-lines basis) and page switching without changing the content of DDRAM as shown below.

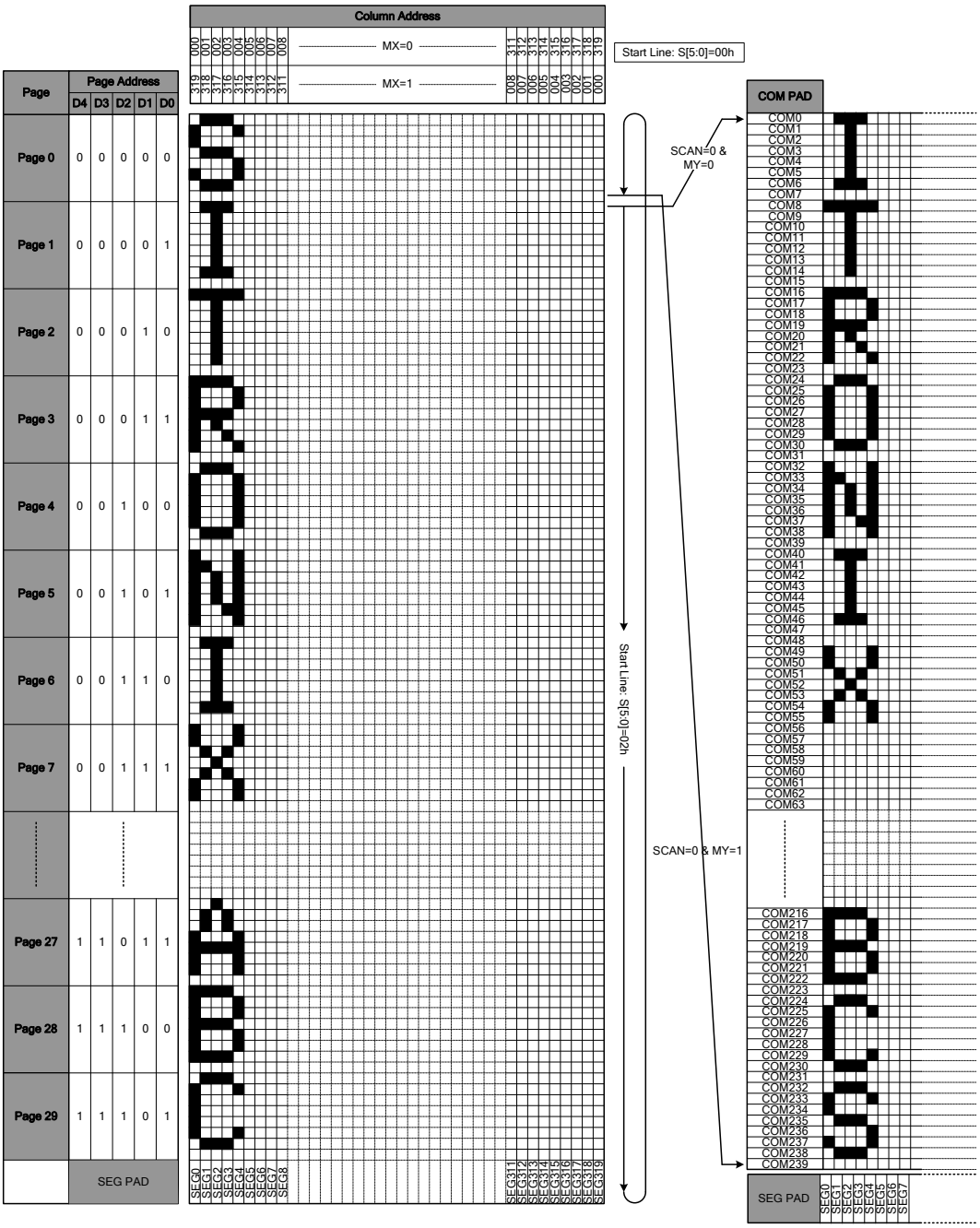


Figure 16 Display Data RAM Map (1/240 Duty)

7.4 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

7.4.1 Internal Analog Power Circuits and External Connection

The maximum external components are 18 capacitors. The detailed values of these capacitors are determined by panel size and panel loading.

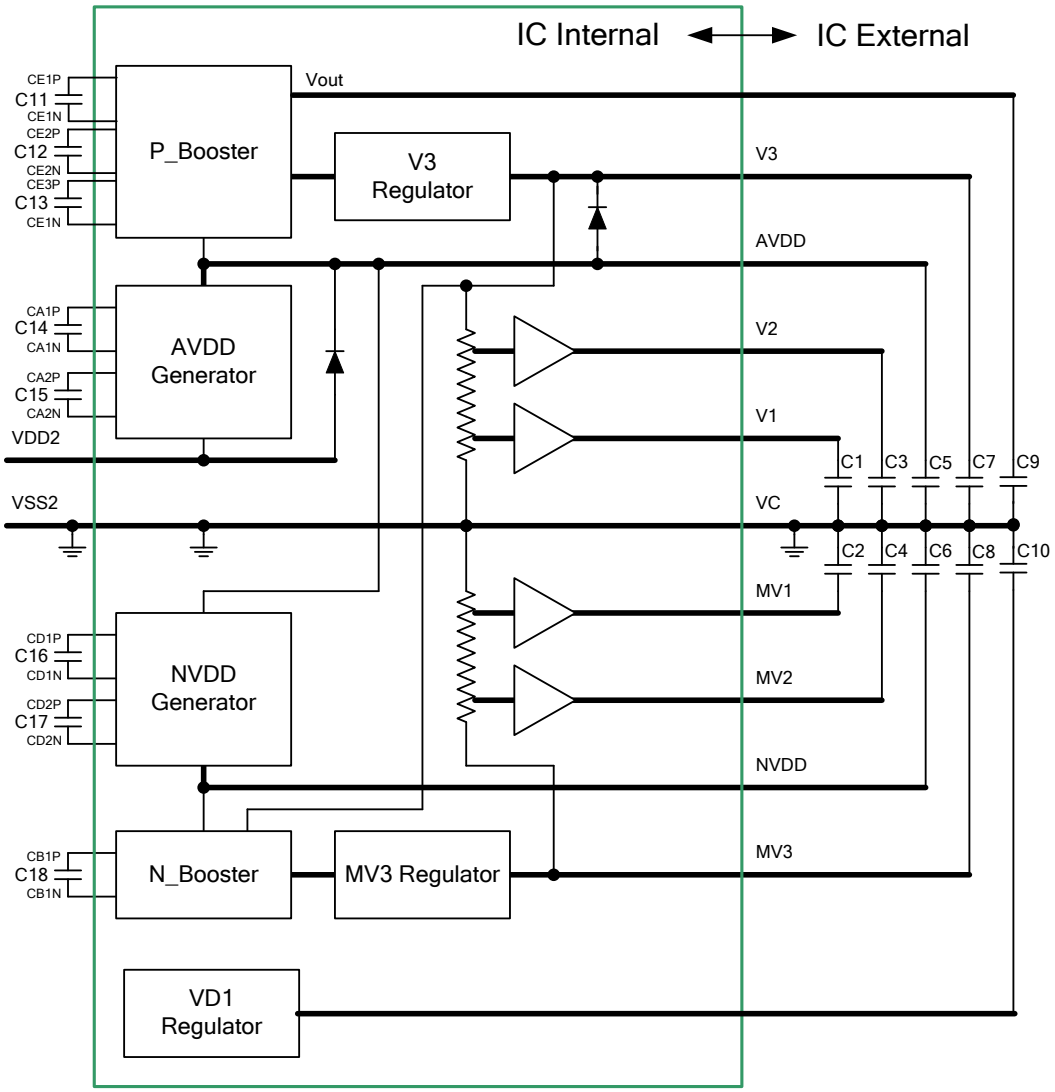


Figure 17 Internal Power Circuits & External Connection

Note : The recommended external power components as below:

C1~C6 : 1uF/10V ~ 4.7uF/10V (Default 1uF/10V)

C7~C9 : 1uF/25V ~ 4.7uF/25V (Default 1uF/25V)

C10~C17 : 1uF/10V ~ 4.7uF/10V (Default 1uF/10V)

C18 : 1uF/25V ~ 4.7uF/25V (Default 1uF/25V)

7.4.2 Voltage Regulator Circuits

The internal voltage regulator circuit provides the liquid crystal operating voltage (Vop) by adjusting register (EV[9:0]). The Vop calculation formula is shown below:

Vop = V3 - MV3 = (5.0 + 0.02 x EV[9:0]) – (-5.0 - 0.02 x EV[9:0])

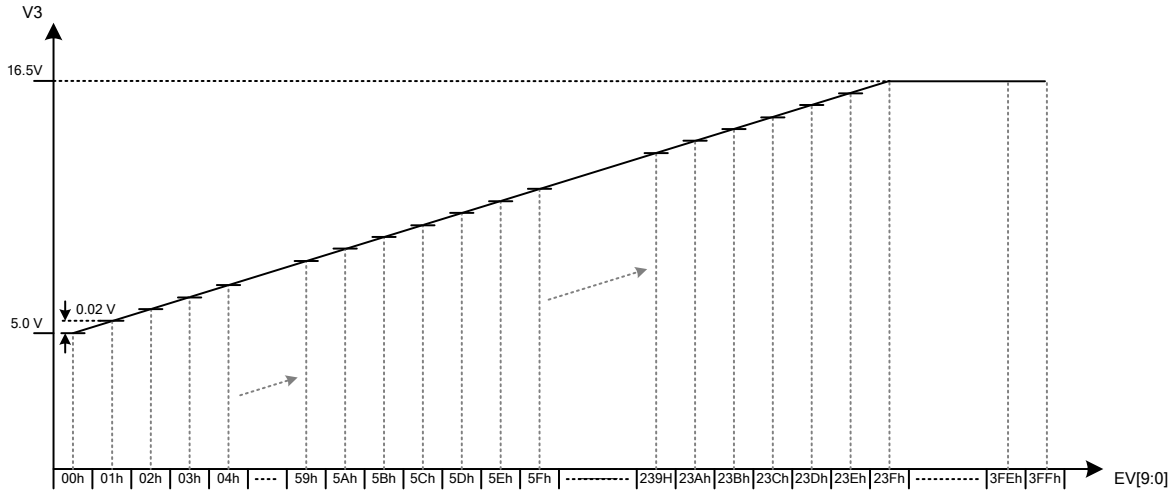


Figure 18 Vop Programmable Range

7.4.3 BIAS Voltage Follower

The internal bias ratio resistors divide V3 and MV3 into four reference levels for V2, V1, MV1 and MV2. The BIAS Voltage Follower generates V2, V1, MV1 and MV2 according to these four reference levels. This circuit is operated in AVDD and NVDD voltage system as the power source. The idea BIAS ratio is shown in below formula:

Idea BIAS ratio: BIAS=(Duty)$^{0.5}$

The available range for V2, V1, MV1 and MV2 is shown in below table.

Symbol	Available Range
V2	2.0V< V2 < AVDD-0.3
V1	1.0V < V1 < V2
MV1	MV2 < MV1< -1.0V
MV2	NVDD+0.7 < MV2 < -2.0V

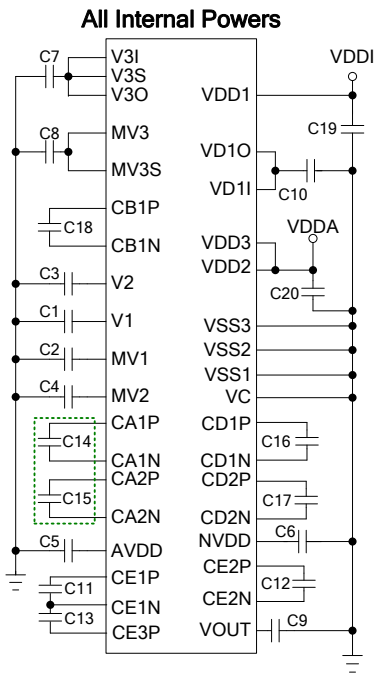
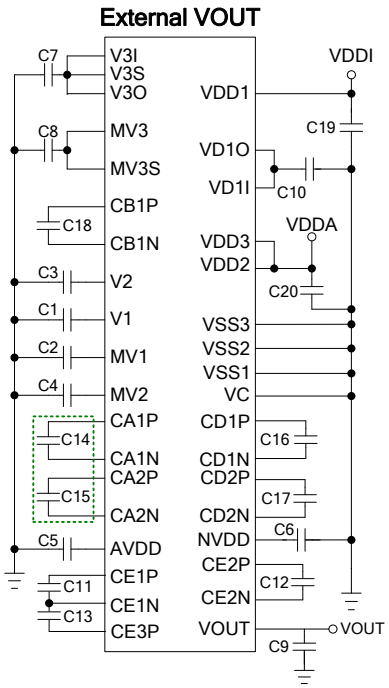
The bias ratio and available V3, MV3 and Vop are shown in below table.

BIAS	Available V3 Range	Available MV3 Range	Available Vop Range
1/6	5.0V ~ 7.05V	-7.05V ~ -5.0V	10.0V ~ 14.1V
1/7	5.0V ~ 8.225V	-8.225V ~ -5.0V	10.0V ~ 16.45V
1/8	5.0V ~ 9.4V	-9.4V ~ -5.0V	10.0V ~ 18.8V
1/9	5.0V ~ 10.575V	-10.575V ~ -5.0V	10.0V ~ 21.15V
1/10	5.0V ~ 11.75V	-11.75V ~ -5.0V	10.0V ~ 23.5V
1/11	5.5V ~ 12.925V	-12.925V ~ -5.5V	11.0V ~ 25.85V
1/12	6.0V ~ 14.1V	-14.1V ~ -6V	12.0V ~ 28.2V
1/13	6.5V ~ 15.275V	-15.275V ~ -6.5V	13.0V ~ 30.55V
1/14	7.0V ~ 16.45V	-16.45V ~ -7.0V	14.0V ~ 32.9V
1/15	7.5V ~ 16.5V	-16.5V ~ -7.5V	15.0V ~ 33V
1/16	8.0V ~ 16.5V	-16.5V ~ -8.0V	16.0V ~ 33V

Note:

1. The maximum voltage level of V3 or minimum voltage level of MV3 that can be generated is dependent on the VDD2, AVDD and the loading of LCD module.
2. The upper limit of the available Vop is absolutely voltage level without consider temperature compensation for V3 and MV3. The voltage level of Vop must be within “Available Vop Range” after considering temperature compensation for V3 and MV3.

The following figures illustrate the connection of typical power applications.

Case 1: All Internal LCD Power Circuits	Case 2: External Regulator (VOUT)
[Hardware Connection] 	**[Hardware Connection]** 
[Software Setting] Power Control: VOUT=V3=VAD=VPF=VMV3=VNAD=VNF=1 **[Related Features]** Contrast Control: Software Control BIAS Control: Software Control Vop Temperature Compensation: Software Defined fFR Temperature Compensation: Software Defined	**[Software Setting]** Power Control: V3=VAD=VPF=VMV3=VNAD=VNF=1, VOUT=0 **[Related Features]** Contrast Control: Software Control BIAS Control: Software Control Vop Temperature Compensation: Software Defined fFR Temperature Compensation: Software Defined

Note :

1. The optimum values of capacitors depend on the loading of LCD panel. The value should be determined by customer. When determining the capacitor value, customer can display a pattern with large loading and than check if the capacitor makes the voltage stable or not.
2. Please place all these capacitors close to the related pin of IC.
3. If the LCD panel is large or the ITO resistance is not good, the capacitor value maybe large than the reference value. If the value is more than 10uF, customer should consider the following suggestion.
4. When the LCD panel size is large and desired display quality is unavailable by increasing the value of capacitor, it is recommended to use the LCD related power externally.
5. The acceptable voltage level of each capacitor as shown in Application Circuit.

7.5 Temperature Gradient Selection Circuit

7.5.1 Set V3 with Temperature Compensation (Temperature ≠ 24°C)

There are 19-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8°C. Please see Figure 19 as below.

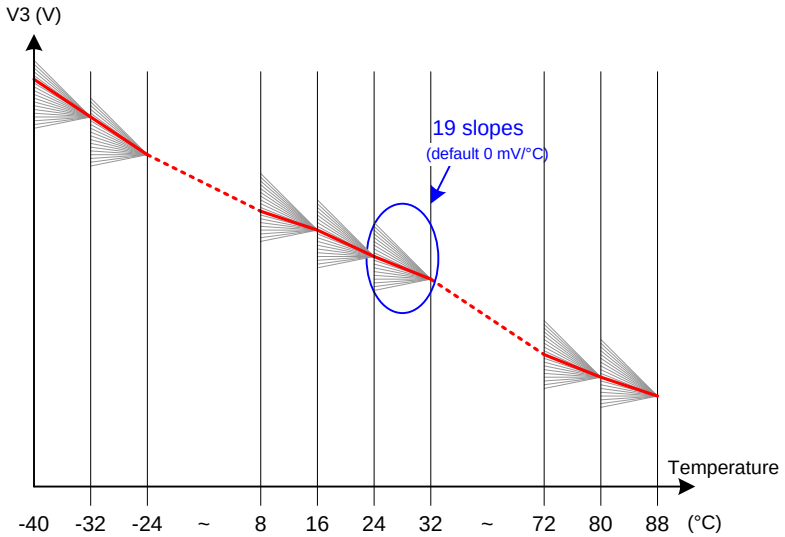


Figure 19 Temperature Compensation Coefficient Selection

The temperature compensation circuit includes negative and positive temperature gradient slope coefficient. If the temperature gradient slope coefficient is negative (FMTx=0), the available gradient Mx is 0mV/°C, -5 mV/°C, -10 mV/°C, … and -75 mV/°C. The parameter (MTx) of Temperature Gradient Set instruction where x=0, 1, 2, …, E, F has a setting value between 0 and 15. MTx=0 results in Mx=0 mV/°C increment on V3, MTx=1 results in Mx=-5 mV/°C increment, …, MTx=15 results in Mx=15x(-5) mV/°C increment. If the temperature gradient slope coefficient is positive (FMTx=1), the available gradient Mx is 0mV/°C, 5 mV/°C, 10 mV/°C and 15 mV/°C. The parameter (MTx) of Temperature Gradient Set instruction where x=0, 1, 2, …, E, F has a setting value between 0 and 3. MTx=0 results in Mx=0 mV/°C decrement on V3, MTx=1 results in Mx=5 mV/°C increment, MTx=2 results in Mx=10 mV/°C increment and MTx=3 results in Mx=15 mV/°C increment.
Note that each MTx individually corresponds to a temperature interval; the Mx means temperature gradient slope coefficient. The relations between Mx and V3 quantity due to temperature V3(T) are described in the equation shown in Table 3.

Temperature Range	Equation V0(T) at temperature=T°C
-40°C ≤ T < -32°C	V3(T) = V3(T24) + (-32 - T) x M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) x 8
-32°C ≤ T < -24°C	V3(T) = V3(T24) + (-24 - T) x M1 + (M2 + M3 + M4 + M5 + M6 + M7) x 8
-24°C ≤ T < -16°C	V3(T) = V3(T24) + (-16 - T) x M2 + (M3 + M4 + M5 + M6 + M7) x 8
-16°C ≤ T < -8°C	V3(T) = V3(T24) + (-8 - T) x M3 + (M4 + M5 + M6 + M7) x 8
-8°C ≤ T < 0°C	V3(T) = V3(T24) + (0 - T) x M4 + (M5 + M6 + M7) x 8
0°C ≤ T < 8°C	V3(T) = V3(T24) + (8 - T) x M5 + (M6 + M7) x 8
8°C ≤ T < 16°C	V3(T) = V3(T24) + (16 - T) x M6 + M7 x 8
16°C ≤ T < 24°C	V3(T) = V3(T24) + (24 - T) x M7
24°C ≤ T < 32°C	V3(T) = V3(T24) - (T - 24) x M8
32°C ≤ T < 40°C	V3(T) = V3(T24) - (T - 32) x M9 - M8 x 8
40°C ≤ T < 48°C	V3(T) = V3(T24) - (T - 40) x MA - (M9 + M8) x 8
48°C ≤ T < 56°C	V3(T) = V3(T24) - (T - 48) x MB - (MA + M9 + M8) x 8
56°C ≤ T < 64°C	V3(T) = V3(T24) - (T - 56) x MC - (MB + MA + M9 + M8) x 8
64°C ≤ T < 72°C	V3(T) = V3(T24) - (T - 64) x MD - (MC + MB + MA + M9 + M8) x 8
72°C ≤ T < 80°C	V3(T) = V3(T24) - (T - 72) x ME - (MD + MC + MB + MA + M9 + M8) x 8
80°C ≤ T < 88°C	V3(T) = V3(T24) - (T - 80) x MF - (ME + MD + MC + MB + MA + M9 + M8) x 8

Table 3 Temperature Gradient Range

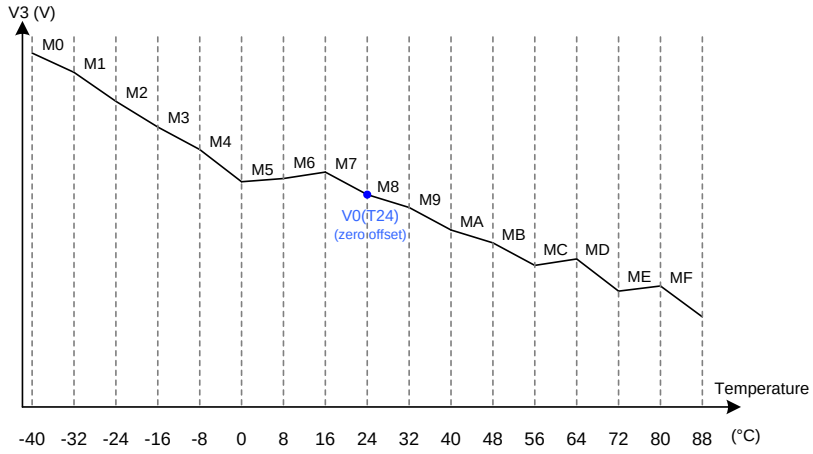


Figure 20 Temperature Gradient Compensation

Note:

- Please make sure to avoid any kind of heating source near ST75320 such as back light, to prevent V3 is not anticipative because of temperature compensation circuit is working.

7.6 Frequency Temperature Gradient Compensation Coefficient

ST75320 will auto-switch frame rate in different temperature such as Fig. 21 . TA, TB and TC are frame rate switching temperature which can be defined by customer with instruction Set Frequency Compensation Temperature Range. FRA, FRB, FRC and FRD are switched frame rate which also can be defined by customer with instruction Operation Clock Frequency Select. The temperature hysteresis “THF” in the Fig 21. that defines the sensitivity of internal temperature sensor and the value can be altered by instruction Temperature Hysteresis Value Set.

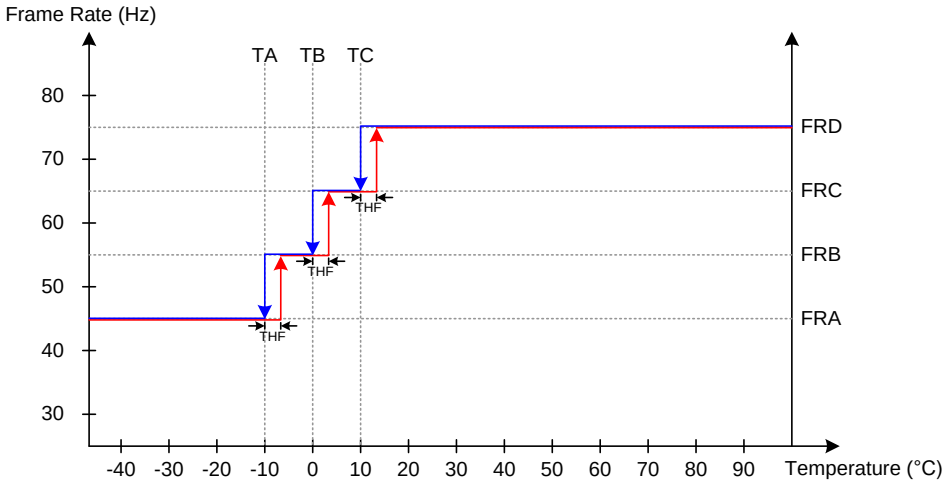


Figure 21 Frame Rate

8 Reset circuit

Setting RSTB pin to “L” (hardware reset) can initialize internal function. The hardware reset is required to initialize internal registers after VDD1 is stable. Initialization by RSTB pin is essential before operating. The default values of registers are listed below:

Procedure	After Hardware Reset
Content of DDRAM	No Change
Display ON/OFF	D=0
Display Inverse	INV=0
Display All Pixel ON	AP=0
COM Output Status	SCAN=0; MY=0
Display Start Line	S[5:0]=00h
Page Address	Y[5:0]=00h
Column Address	X[8:0]=000h
Display Data Input/Output Direction	DIR=0
Column Address Direction	MX=0
N-Line Inversion	NL[5:0]=00h
N-Line Inversion ON/FF	NL=0
Display Area	DTY[2:0]=07h, SP[5:0]=00h
Built-in Oscillator Circuit ON/OFF	OSC=0
Operation Clock Frequency	FRA[3:0]=05h; FRB[3:0]=05h; FRC[3:0]=05h; FRD[3:0]=05h
Power Control	VOUT=0; VAD=0; V3=0; VPF=0; VMV3=0; VNAD=0; VNF=0
Frame Rate Level	DBL=0
BIAS	BS[3:0]=09h
Electronic Volume	EV[9:0]=00h
Power Discharge	DV3=0; DVPF=0; DVNF=0; DVMV3=0
Power Save	PD=1
Temperature Gradient Compensation	MT0[3:0]=00h; MT1[3:0]=00h; MT2[3:0]=00h; MT3[3:0]=00h; MT4[3:0]=00h; MT5[3:0]=00h; MT6[3:0]=00h; MT7[3:0]=00h; MT8[3:0]=00h; MT9[3:0]=00h; MTA[3:0]=00h; MTB[3:0]=00h; MTC[3:0]=00h; MTD[3:0]=00h; MTE[3:0]=00h; MTF[3:0]=00h;
Temperature Gradient Compensation Flag	FMT[15:0]=0000h
LCD Driving Method	NLFR=0
Frequency Compensation Temperature Range	TA[6:0]=00h, TB[6:0]=00h, TC[6:0]=00h
Temperature Hysteresis Value	THV[5:0]=04h, THF[3:0]=02h

Table 4 Reset Register Table

9 COMMAND

9.1 INSTRUCTION TABLE

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	Set LCD display mode D=0: display off D=1: display on
Display Inverse	0	0	1	0	1	0	0	1	1	INV	Set inverse display mode INV=0: normal display INV=1: inverse display
Display All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all pixel on mode AP=0: normal display AP=1: all pixel on
COM Output Status	0	0	1	1	0	0	0	1	0	0	Set COM output mode SCAN=0: normal scan SCAN=1: interlace scan MY=0: COM0→COM239 MY=1: COM239→COM0
	1	0	-	-	-	-	-	0	SCAN	MY	
Display Start Line	0	0	1	0	0	0	1	0	1	0	Set display start line
	1	0	-	-	S5	S4	S3	S2	S1	S0	
Page Address	0	0	1	0	1	1	0	0	0	1	Set the page address of DDRAM
	1	0	-	-	Y5	Y4	Y3	Y2	Y1	Y0	
Column Address	0	0	0	0	0	1	0	0	1	1	Set the column address of DDRAM
	1	0	-	-	-	-	-	-	-	X8	
	1	0	X7	X6	X5	X4	X3	X2	X1	X0	
Display Data Write	0	0	0	0	0	1	1	1	0	1	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Read	0	0	0	0	0	1	1	1	0	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Input/Output Direction	0	0	1	0	0	0	0	1	0	DIR	Set DDRAM data input direction DIR=0: column direction DIR=1: page direction
Column Address Direction	0	0	1	0	1	0	0	0	0	MX	Set column addressing direction MX=0: COL-0→ COL-319 MX=1: COL-319→ COL-0
N-Line Inversion	0	0	0	0	1	1	0	1	1	0	Set N-Line inversion
	1	0	-	-	NL5	NL4	NL3	NL2	NL1	NL0	

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
N-Line Inversion ON/OFF	0	0	1	1	1	0	0	1	0	NL	Set N-Line inversion mode NL=0:N-Line inversion off NL=1:N-Line inversion on
Display Area	0	0	0	1	1	0	1	1	0	1	Set the display area DTY[2:0]=00h~07h SP[5:0]=00h~4Fh
	1	0	-	-	-	-	-	DTY2	DTY1	DTY0	
	1	0	-	-	SP5	SP4	SP3	SP2	SP1	SP0	
Read Modify Write	0	0	1	1	1	0	0	0	0	0	Enable Read Modify Write mode
Read Modify Write End	0	0	1	1	1	0	1	1	1	0	Disable Read Modify Write mode
Built-in Oscillator Circuit ON/OFF	0	0	1	0	1	0	1	0	1	OSC	Set built-in oscillator mode OSC=0: built-in oscillator off OSC=1: built-in oscillator on
Operation Clock Frequency	0	0	0	1	0	1	1	1	1	1	Set frame rate in different temperature range
	1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
	1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	
Power Control	0	0	0	0	1	0	0	1	0	1	Set built-in power circuits on/off
	1	0	-	VOUT	VAD	V3	VPF	VMV3	VNAD	VNF	
Frame Rate Level	0	0	0	0	1	0	1	0	1	1	Set the level of frame rate
	1	0	-	-	-	-	-	-	-	DBL	
BIAS	0	0	1	0	1	0	0	0	1	0	Set the bias ratio of liquid crystal driving voltage
	1	0	-	-	-	-	BS3	BS2	BS1	BS0	
Electronic Volume	0	0	1	0	0	0	0	0	0	1	Set the V3 level for liquid crystal driving voltage
	1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
	1	0	-	-	-	-	-	-	EV9	EV8	
Power Discharge	0	0	1	1	1	0	1	0	1	0	Set power circuits discharge.
	1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	
Power Save	0	0	1	0	1	0	1	0	0	PD	Set power save mode PD=0: normal mode PD=1: standby mode

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Gradient Compensation	0	0	0	1	0	0	1	1	1	0	Set temperature gradient compensation coefficient
	1	0	MT1[3:0]				MT0[3:0]				
	1	0	MT3[3:0]				MT2[3:0]				
	1	0	MT5[3:0]				MT4[3:0]				
	1	0	MT7[3:0]				MT6[3:0]				
	1	0	MT9[3:0]				MT8[3:0]				
	1	0	MTB[3:0]				MTA[3:0]				
	1	0	MTD[3:0]				MTC[3:0]				
	1	0	MTF[3:0]				MTE[3:0]				
Temperature Gradient Compensation Flag	0	0	0	0	1	1	1	0	0	1	Set the slope of temperature gradient is positive or negative
	1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
	1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	
Read Status	0	0	1	0	0	0	1	1	1	0	Read IC status
	1	1	D	OSC	AVD	V3	VFP	VMV3	VNAD	VFN	
	1	1	DISV	ITR	MY	PD	TD	NLFR	MLS	-	
Temperature Detection	0	0	0	1	1	0	1	0	0	TD	Set temperature detection mode TD=0: disable mode TD=1: enable mode
LCD Driving Method	0	0	1	1	1	0	0	1	1	1	Set LCD driving method
	1	0	0	0	0	NLFR	1	0	0	1	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Frequency Compensation Temperature Range	0	0	1	1	1	0	1	1	0	0	Set temperature range for frequency compensation
	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
Temperature Hysteresis Value	0	0	1	1	1	0	1	1	0	1	Set temperature hysteresis value
	1	0	-	-	THV5	THV4	THV3	THV2	THV1	THV0	
	1	0	-	-	-	-	THF3	THF2	THF1	THF0	
Current Temperature Data	0	0	1	1	1	0	1	1	1	1	Monitor current temperature
	1	1	T7	T6	T5	T4	T3	T2	T1	T0	
Read ID	0	0	1	0	0	0	1	1	1	1	Read ID value
	1	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	

COMMAND TABLE										
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE							DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode TE=0: normal command mode TE=1: test command mode T: select test command mode

Note:

1. “-” is disable bit. It can be either logic 0 or 1.
2. Do NOT use non-specified instructions in any extension command mode.

9.2 INSTRUCTION DESCRIPTION

9.2.1 Display ON/OFF

This instruction turns the display ON or OFF. When ST75320 enters display off, the display output is blank regardless of the content of DDRAM. When ST75320 enters display on (exit display off), the display output is according to content of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	1	1	D	D=0: Display off D=1: Display on

9.2.2 Display Inverse

This instruction would inverse the scanned data without recover the content of DDRAM. As the result, the ON and OFF status of all pixels are interchanged.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	1	INV	INV=0: Normal display INV=1: Inverse display

9.2.3 Display All Pixel ON

When ST75320 enters all pixels on mode, all display pixels are turned on regardless of the content of DDRAM. The content of DDRAM is not changed by setting Display All Pixel ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	0	AP	AP=0: Normal display AP=1: All pixel on

9.2.4 COM Output Status

This instruction defines the COM scan method and the direction of scan read from DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	1	0	0	SCAN=0: Normal scan SCAN=1 :Interlace Scan Interlace
1	0	-	-	-	-	-	-	SCAN	MY	MY=0: COM0→COM239 MY=1: COM239→COM0

Note: "-" is disable bit. It can be either logic 0 or 1.

9.2.5 Display Start Line

This instruction sets the display start line address of DDRAM shown in Figure 16. The display data of specified display start line address is displayed at the start point (start point is specified by instruction Display Area). Continuously increasing or decreasing the start line address results in vertical-scrolling in 4-line basis. The detail description is showed in the section of Line Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	1	0	1	0	S[5:0]=00h~3Bh
1	0	-	-	S5	S4	S3	S2	S1	S0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter S[5:0] and the line address of DDRAM is shown below.

S5	S4	S3	S2	S1	S0	Line Address of DDRAM
0	0	0	0	0	0	0 x 4 = 0
0	0	0	0	0	1	1 x 4 = 4
0	0	0	0	1	0	2 x 4 = 8
:	:	:	:	:	:	:
1	1	1	0	0	1	57 x 4 = 228
1	1	1	0	1	0	58 x 4 = 232
1	1	1	0	1	1	59 x 4 = 236

9.2.6 Page Address

This instruction defines the page address corresponding to line address of DDRAM when MCU access to the DDRAM shown in Figure 15. The detail description is showed in the section of Page address circuit

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	0	0	1	Y[5:0]=00h~1Dh
1	0	-	-	Y5	Y4	Y3	Y2	Y1	Y0	

Note: "-" is disable bit. It can be either logic 0 or 1.

Y5	Y4	Y3	Y2	Y1	Y0	Page Address
0	0	0	0	0	0	Page 0
0	0	0	0	0	1	Page 1
0	0	0	0	1	0	Page 2
:	:	:	:	:	:	:
0	1	1	0	1	1	Page 27
0	1	1	1	0	0	Page 28
0	1	1	1	0	1	Page 29

9.2.7 Column Address

This instruction defines the column address of DDRAM. The detail description is showed in the section of Column Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	0	1	1	X[8:0]=000h~13Fh
1	0	-	-	-	-	-	-	-	X8	
1	0	X7	X6	X5	X4	X3	X2	X1	X0	

Note: "-" is disable bit. It can be either logic 0 or 1.

X8	X7	X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	0	0	1	Column 1
0	0	0	0	0	0	0	1	0	Column 2
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	1	Column 317
1	0	0	1	1	1	1	1	0	Column 318
1	0	0	1	1	1	1	1	1	Column 319

9.2.8 Display Data Write

This instruction is used to transfer data from MCU to DDRAM without changing status of ST75320. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter write DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Display Data Write would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	1	
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

9.2.9 Display Data Read

The instruction is used to transfer data from DDRAM to MCU without changing status of ST75320. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter read DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Read Display Data would be stopped when any other instruction is accepted. Read Display Data is only available via the parallel interface.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	0	
1	1	D7	D6	D5	D4	D3	D2	D1	D0	

9.2.10 Display Data Input/Output Direction

This instruction defines the direction where the address counter of DDRAM is automatically increment.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	1	0	DIR	DIR=0: Column direction DIR=1: Page direction

9.2.11 Column Address Direction

This instruction defines the addressing direction of column address as shown in Figure 15.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	0	MX	MX=0: COL-0→ COL-319 MX=1: COL-319→ COL-0

9.2.12 N-Line Inversion

This instruction defines the liquid crystal alternating line number which alters the driving signal phase (in 4-line basis).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	1	1	0	NL[5:0]=00h~2Ch
1	0	-	-	NL5	NL4	NL3	NL2	NL1	NL0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter NL[5:0] and the number of inverted lines is shown below.

NL5	NL4	NL3	NL2	NL1	NL0	N-Line Inversion
0	0	0	0	0	0	8 (4x2)
0	0	0	0	0	1	8 (4x2)
0	0	0	0	1	0	12 (4x3)
:	:	:	:	:	:	:
1	1	1	0	0	0	228 (4x57)
1	1	1	0	0	1	232 (4x58)
1	1	1	0	1	0	236 (4x59)

9.2.13 N-Line Inversion ON/OFF

This instruction defines the function of N-Line inversion is disable or enable. If the N-Line inversion is turning off, the liquid crystal is alternated by frame inversion.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	NL	NL=0: N-Line inversion off NL=1: N-Line inversion on

9.2.14 Display Area

This instruction defines the display duty and the start point (in 4-line basis). The display duty is specified the number of display line in 4-line basis. The start point is specified the first output COM number that mapping to Display Start Line of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	1	0	1	DTY[2:0]=00h~07h SP[5:0]=00h~3Bh
1	0	-	-	-	-	-	DTY2	DTY1	DTY0	
1	0	-	-	SP5	SP4	SP3	SP2	SP1	SP0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter DTY[2:0] and the number of display lines is shown below.

DTY2	DTY1	DTY0	Scan Duty
0	0	0	1/32
0	0	1	1/64
0	1	0	1/96
0	1	1	1/120
1	0	0	1/128
1	0	1	1/160
1	1	0	1/192
1	1	1	1/240

The relationship between the parameter SP[5:0] and the start point is shown below.

SP5	SP4	SP3	SP2	SP1	SP0	Start Point
0	0	0	0	0	0	0 (COM0~COM3)
0	0	0	0	0	1	1 (COM4~COM7)
0	0	0	0	1	0	2 (COM8~COM11)
:	:	:	:	:	:	:
1	1	1	0	0	1	57 (COM228~COM231)
1	1	1	0	1	0	58 (COM232~COM235)
1	1	1	0	1	1	59 (COM236~COM239)

9.2.15 Read Modify Write

This instruction is used to enter Read Modify Write mode. When entering Read Modify Write mode, the display data read will not increase address counter. Only the display data write will increase the address counter. This mode is maintained until the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	

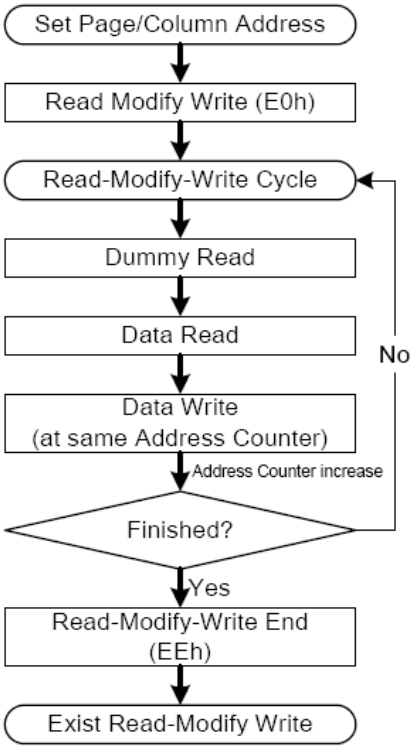


Figure 22 Read Modify Write Flow

9.2.16 Read Modify Write End

This instruction is used to release the Read Modify Write mode. The page address and column address will return to initial address while the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	0	

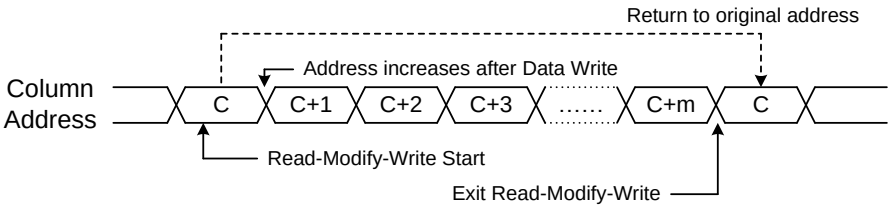


Figure 23 Address Relationship of Read Modify Write

9.2.17 Built-in Oscillator Circuit ON/OFF

This instruction is used to turn on or off the built-in oscillator circuit. When the built-in power supply is used, the Built-in Oscillator Circuit ON must be executed before the instruction Power Control. If the built-in oscillator circuit is turned off while the built-in power supply is used, abnormal display may occur.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	OSC	OSC=0: Built-in oscillator off OSC=1: Built-in oscillator on

9.2.18 Operation Clock Frequency

This instruction defines the temperature compensation gradient of frequency which automatically adjusts the frame frequency according to the current temperature.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	1	1	FRA[3:0]: FR for -40°C~TA FRB[3:0]: FR for TA~TB FRC[3:0]: FR for TB~TC FRD[3:0]: FR for TC~88°C
1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	

FRx[3:0]	Frame Rate (DBL = 0)
0000	143
0001	117
0010	98
0011	80
0100	72
0101	62
0110	58
0111	54
1000	48
1001	44
1010	40
1011	38
1100	36
1101	34
1110	12
1111	5

FRx[3:0]	Frame Rate (DBL = 1)
0000	286
0001	234
0010	198
0011	161
0100	143
0101	123
0110	117
0111	107
1000	95
1001	87
1010	81
1011	78
1100	72
1101	67
1110	24
1111	10

9.2.19 Power Control

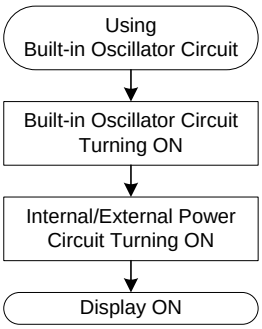
This instruction used to control the status of built-in power circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	1	0	1	
1	0	-	VOUT	VAD	V3	VPF	VMV3	VNAD	VNF	

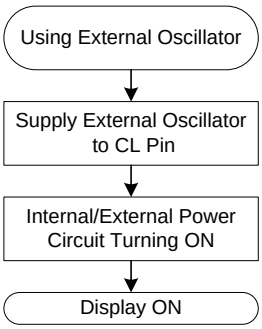
Note: "-" is disable bit. It can be either logic 0 or 1.

Flag	Status of Built-in Power Circuit
VOUT	VOUT=0: Built-in VOUT Booster Circuit OFF VOUT=1: Built-in VOUT Booster Circuit ON
VAD	VAD=0: Built-in AVDD Booster Circuit OFF VAD=1: Built-in AVDD Booster Circuit ON
V3	V3=0: Built-in V3 Regulator Circuit OFF V3=1: Built-in V3 Regulator Circuit ON
VPF	VPF=0: Built-in Positive Follower Circuit OFF VPF=1: Built-in Positive Follower Circuit ON
VMV3	VMV3=0: Built-in MV3 Regulator Circuit OFF VMV3=1: Built-in MV3 Regulator Circuit ON
VNAD	VNAD=0: Built-in NAVDD Booster Circuit OFF VNAD=1: Built-in NAVDD Booster Circuit ON
VNF	VNF=0: Built-in Negative Follower Circuit OFF VNF=1: Built-in Negative Follower Circuit ON

The internal clock is required to operate the built-in power supply circuit. During the operation of the built-in power supply circuit, be sure that the internal clock is present inside. If the built-in oscillator circuit is used, please execute the built-in oscillator circuit turning on before the power circuit turning on. If the external oscillator is used, must operate the external oscillator before the power circuit turning on. If the internal clock is cut off during the operation of the built-in power circuit, abnormal display mat occur.



Power Control (Using Built-in Oscillator)



Power Control (Using External Oscillator)

9.2.20 Frame Rate Level

This instruction defines the frame rate level without change any hardware connection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	0	1	1	DBL=0: x1
1	0	-	-	-	-	-	-	-	DBL	DBL=1: x2

Note: "-" is disable bit. It can be either logic 0 or 1.

9.2.21 BIAS

This instruction defines the bias ratio of voltage requirement for liquid crystal.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	1	0	
1	0	-	-	-	-	BS3	BS2	BS1	BS0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter BS[3:0] and the bias ratio is shown below.

BS3	BS2	BS1	BS0	BIAS Ratio
0	0	0	0	1/6
0	0	0	1	1/7
0	0	1	0	1/8
0	0	1	1	1/9
0	1	0	0	1/10
0	1	0	1	1/11
0	1	1	0	1/12
0	1	1	1	1/13
1	0	0	0	1/14
1	0	0	1	1/15
1	0	1	0	1/16

The relationship between the bias ratio and the analog voltage level is shown below.

Symbol	Voltage Level
V3	V3 = Vop/2
V2	V2 = 2 x BIAS x Vop
V1	V1 = BIAS x Vop
VC	VC = VSS2
MV1	MV1 = -BIAS x Vop
MV2	MV2 = -2 x BIAS x Vop
MV3	MV3 = -Vop/2

Note: The limitation of analog voltage is shown in section of BIAS Voltage Follower.

9.2.22 Electronic Volume

This instruction defines the liquid crystal driving voltage V3 that issued from built-in analog power circuit. The maximum voltage level of Vop that can be generated is dependent on the VDD2 voltage and the loading of LCD module. The detail description is showed in section of Voltage Regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	0	0	1	EV[9:0]=00h~23Fh
1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
1	0	-	-	-	-	-	-	EV9	EV8	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter EV[9:0] and the voltage level of V3/MV3/Vop is shown below.

EV9	EV8	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	V3	MV3	Vop
0	0	0	0	0	0	0	0	0	0	5.00	-5.00	10
0	0	0	0	0	0	0	0	0	1	5.02	-5.02	10.04
0	0	0	0	0	0	0	0	1	0	5.04	-5.04	10.08
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	1	1	1	1	0	1	16.46	-16.46	32.92
1	0	0	0	1	1	1	1	1	0	16.48	-16.48	32.96
1	0	0	0	1	1	1	1	1	1	16.50	-16.50	33.00
1	0	0	1	0	0	0	0	0	0	16.50	-16.50	33.00
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	1	1	1	1	1	1	16.50	-16.50	33.00

Note: The formula of idea Vop is shown in section of Voltage Regulator.

9.2.23 Power Discharge

This instruction used to discharge the capacitor connected to the analog power supply circuit. The discharge flow please refers to the sections of Power OFF to avoid abnormal display.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	0	1	0	
1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	

Flag	Status of Built-in Power Circuit
DV3	DV3=0: Disable discharge V3 DV3=1: Enable discharge V3
DVPF	DVPF=0: Disable discharge positive follower (V2 & V1) DVPF=1: Enable discharge positive follower (V2 & V1)
DVNF	DVNF=0: Disable discharge negative follower (MV1 & MV2) and NAVDD DVNF=1: Enable discharge negative follower (MV1 & MV2) and NAVDD
DVMV3	DVMV3=0: Disable discharge MV3 DVMV3=1: Enable discharge MV3

Note:

1. Do not discharge before related power is turned off while using internal power system.
2. Do not discharge before related power is turned off while using external power system.

9.2.24 Power Save

This instruction defines the status of chip is normal mode or standby mode. When ST75320 enters the standby mode, the mode causes the LCD module entering the minimum power consumption. Besides, the internal analog circuit will be turned off without discharge power and the display will turn off.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	PD	PD=0: Normal mode PD=1: Standby mode

9.2.25 Temperature Gradient Compensation

This instruction defines the temperature gradient compensation coefficient. Depend on the instruction of Temperature Gradient Compensation Flag, the temperature gradient slope can be set either positive or negative. The detail description is showed in the section of Temperature Gradient Selection Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	1	1	1	0	MTx[3:0]=0h~Fh (Negative TC) MTx[3:0]=0h~3h (Positive TC)
1	0	MT1[3:0]				MT0[3:0]				
1	0	MT3[3:0]				MT2[3:0]				
1	0	MT5[3:0]				MT4[3:0]				
1	0	MT7[3:0]				MT6[3:0]				
1	0	MT9[3:0]				MT8[3:0]				
1	0	MTB[3:0]				MTA[3:0]				
1	0	MTD[3:0]				MTC[3:0]				
1	0	MTF[3:0]				MTE[3:0]				

The related temperature range and available setting value of MTx[3:0] is shown below.

Flag	Temperature Range	Negative TC Value	Positive TC Value
MT0[3:0]	-40°C ≤ T < -32°C	0h~Fh	0h~3h
MT1[3:0]	-32°C ≤ T < -24°C	0h~Fh	0h~3h
MT2[3:0]	-24°C ≤ T < -16°C	0h~Fh	0h~3h
MT3[3:0]	-16°C ≤ T < -8°C	0h~Fh	0h~3h
MT4[3:0]	-8°C ≤ T < 0°C	0h~Fh	0h~3h
MT5[3:0]	0°C ≤ T < 8°C	0h~Fh	0h~3h
MT6[3:0]	8°C ≤ T < 16°C	0h~Fh	0h~3h
MT7[3:0]	16°C ≤ T < 24°C	0h~Fh	0h~3h
MT8[3:0]	24°C ≤ T < 32°C	0h~Fh	0h~3h
MT9[3:0]	32°C ≤ T < 40°C	0h~Fh	0h~3h
MTA[3:0]	40°C ≤ T < 48°C	0h~Fh	0h~3h
MTB[3:0]	48°C ≤ T < 56°C	0h~Fh	0h~3h
MTC[3:0]	56°C ≤ T < 64°C	0h~Fh	0h~3h
MTD[3:0]	64°C ≤ T < 72°C	0h~Fh	0h~3h
MTE[3:0]	72°C ≤ T < 80°C	0h~Fh	0h~3h
MTF[3:0]	80°C ≤ T < 88°C	0h~Fh	0h~3h

The relationship between the parameters FMTx/MTx[3:0] and the voltage level of V3/MV3/Vop is shown below. The FMTx is set by instruction of Temperature Gradient Compensation Flag.

FMTx	MTx3	MTx2	MTx1	MTx0	V3(mV/°C)	MV3(mV/°C)	Vop(mV/°C)
0	0	0	0	0	0	0	0
	0	0	0	1	-5	5	-10
	0	0	1	0	-10	10	-20
	0	0	1	1	-15	15	-30
	0	1	0	0	-20	20	-40
	0	1	0	1	-25	25	-50
	0	1	1	0	-30	30	-60
	0	1	1	1	-35	35	-70
	1	0	0	0	-40	40	-80
	1	0	0	1	-45	45	-90
	1	0	1	0	-50	50	-100
	1	0	1	1	-55	55	-110
	1	1	0	0	-60	60	-120
	1	1	0	1	-65	65	-130
	1	1	1	0	-70	70	-140
	1	1	1	1	-75	75	-150
1	0	0	0	0	0	0	0
	0	0	0	1	5	-5	10
	0	0	1	0	10	-10	20
	0	0	1	1	15	-15	30

9.2.26 Temperature Gradient Compensation Flag

This instruction defines the temperature gradient compensation coefficient is negative or positive temperature gradient compensation coefficient.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	1	0	0	1	FMTx=0: Negative TC FMTx=1: Positive TC
1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	

9.2.27 Read Status

This instruction can read out the status of ST7320.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	1	1	1	0	
1	1	D	OSC	AVD	V3	VFP	VMV3	VNAD	VFN	
1	1	DISV	ITR	MY	PD	TD	NLFR	MLS	-	

The relationship between the flag and the status of IC is shown below.

Flag	Function	0	1
D	Display ON/OFF	OFF	ON
OSC	Built-in OSC Circuit ON/OFF	OFF	ON
AVD	AVDD ON/OFF	OFF	ON
V3	V3 ON/OFF	OFF	ON
VFP	Positive Follower ON/OFF	OFF	ON
VMV3	MV3 ON/OFF	OFF	ON
VNAD	NAVDD ON/OFF	OFF	ON
VFN	Negative Follower ON/OFF	OFF	ON
DISV	Power Discharge ON/OFF	OFF	ON
ITR	COM Output Mode	Normal	Interlace
MY	COM Output Direction	Normal	Reverse
PD	Power Save	Normal	Standby
TD	Temperature Detection ON/OFF	OFF	ON
NLFR	N-Line Inversion Reset by Frame ON/OFF	ON	OFF
MLS	MLS Dispersion/Non-dispersion	Dispersion	Non-dispersion

9.2.28 Temperature Detection

This instruction defines the status of temperature detection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	0	0	TD	TD=0 : Disable mode TD=1 : Enable mode

9.2.29 LCD Driving Method

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	1	1	
1	0	0	0	0	NLFR	1	0	0	1	

Note: "-" is disable bit. It can be either logic 0 or 1.

Flag	Status
NLFR	NLFR=0: N-Line Inversion Reset by Frame Inversion ON NLFR=1: N-Line Inversion Reset by Frame Inversion OFF

The relationship between parameters (NL & NLFR) and COM output method is shown below.

A. 20 lines display without N-Line inversion (NL=0, NLFR=x)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			+ + + +					- - - -		
COM[15:12]				+ + + +					- - - -	
COM[19:16]					+ + + +					- - - -

B. 12-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					+ + + +			
COM[11:8]			+ + + +					+ + + +		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					- - - -					- - - -

C. 8-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					+ + + +				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			- - - -					- - - -		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					+ + + +					+ + + +

D. 12-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			+ + + +					- - - -		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					- - - -					+ + + +

E. 8-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			- - - -					+ + + +		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					+ + + +					- - - -

9.2.30 NOP

"No Operation" instruction. ST75320 will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	1	No operation

9.2.31 Frequency Compensation Temperature Range

This instruction defines the temperature range for automatic frame rate adjustment according to current temperature as shown in Figure 21.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	0	TA[6:0]=00h~7Fh TB[6:0]=00h~7Fh TC[6:0]=00h~7Fh
1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The target temperature add 40 will become the decimal value of register TA[6:0]/TB[6:0]/TC[6:0].

Temp. Range Value	Temp. Rising State (°C)	Temp. Falling State (°C)	Restriction
Freq. Changing Point A (TA)	(TA[6:0]-40)+THF[3:0]	TA[6:0]-40	TB[6:0]>TA[6:0]+THF[3:0] TC[6:0]>TB[6:0]+THF[3:0] 87°C ≥ TC[6:0]+THF[3:0]
Freq. Changing Point B (TB)	(TB[6:0]-40)+THF[3:0]	TB[6:0]-40	
Freq. Changing Point C (TC)	(TC[6:0]-40)+THF[3:0]	TC[6:0]-40	

Example:

If TA wants to be set at -10°C, TA[6:0]=-10+40=30=1Eh

If TB wants to be set at 0°C, TB[6:0]=0+40=40=28h

If TC wants to be set at 10°C, TC[6:0]=10+40=50=32h

9.2.32 Temperature Hysteresis Value

This instruction defines the temperature compensation threshold. THV[5:0] is used to set the threshold (hysteresis) value for Vop while THF[3:0] is used to set the threshold (hysteresis) value for frame frequency (fFR). The threshold values (THV & THF) can avoid the Vop/fFR switching up and down, when the ambient temperature changes around the junction of two temperature ranges. When the ambient temperature is decreasing, the Vop/fFR is changed at the junction temperature between two temperature ranges. But if the temperature is increasing, the Vop/fFR is not changed until the temperature exceeds the "junction + hysteresis". For example,

- THV[5:0]=4 (2°C) and the ambient temperature is increasing from 27°C to 35°C. Vop slope is MT8 in 27.0°C ~33.5°C, and it changes to MT9 if Ta is 34°C or higher.
- Similarly, if we set THF[3:0]=3 (3°C) and TA at -20°C as a point to change fFR. fFR changes from FRB[3:0] to FRA[3:0] when temperature decreases from -19.5°C to -20.0°C. But fFR changes from FRA[3:0] to FRB[3:0] when temperature increases from -17.5°C to -17.0°C.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	1	THV[5:0]=00h~3Fh THF[3:0]=00h~0Fh
1	0	-	-	THV5	THV4	THV3	THV2	THV1	THV0	
1	0	-	-	-	-	THF3	THF2	THF1	THF0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter THV[5:0] and the temperature hysteresis for Vop is shown below.

THV5	THV4	THV3	THV2	THV1	THV0	Temp. Hysteresis for Vop
0	0	0	0	0	0	0°C
0	0	0	0	0	1	0.5°C
0	0	0	0	1	0	1.0°C
:	:	:	:	:	:	:
1	1	1	1	0	1	31.5°C
1	1	1	1	1	0	31.0°C
1	1	1	1	1	1	31.5°C

The relationship between the parameter THF[3:0] and the temperature hysteresis for frame rate is shown below.

THF3	THF2	THF1	THF0	Temp. Hysteresis for FR
0	0	0	0	0°C (stop TC auto-adjust of fFR)
0	0	0	1	1°C
0	0	1	0	2°C
:	:	:	:	:
1	1	0	1	13°C
1	1	1	0	14°C
1	1	1	1	15°C

9.2.33 Current Temperature Data

This instruction used to detect current temperature. If the value of T[7:0] is 00h means the internal detected temperature is -40°C **(Temperature=T[7:0]x0.5-40)**. The tolerance of internal detected temperature is depend on the parameter of THV[5:0]. This function is used for Vop and frame rate compensation. It can not used to replace a real temperature sensor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	1	
1	1	T7	T6	T5	T4	T3	T2	T1	T0	

9.2.34 Read ID

This instruction is used to read ID value.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	1	1	1	1	
1	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	

9.2.35 Test

This instruction is reserved for IC testing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	1	1	TE	T	TE=0: Normal command mode TE=1: Test command mode T: Select test command mode

9.3 INSTRUCTION TABLE (PROM Function)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode
TE=1 & T=1											
Vop Increase	0	0	1	1	0	1	0	1	1	0	Vop increase one step
Vop Decrease	0	0	1	1	0	1	0	1	1	1	Vop decrease one step
Vop Offset	0	0	1	1	0	1	0	0	1	1	Vop offset
	1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	
PROM WR/RD Control	0	0	1	0	0	1	0	0	0	1	PROM WR/RD control WR/RD=0: enable PROM read WR/RD=1: enable PROM write
	1	0	0	0	WR /RD	0	0	0	0	0	
PROM Control Out	0	0	1	0	0	1	0	0	1	0	Cancel PROM control function
PROM Write	0	0	1	0	0	1	0	0	1	1	PROM programming procedure
PROM Read	0	0	1	0	0	1	0	1	0	0	PROM up-load procedure
PROM Auto Read Control	0	0	1	0	0	1	0	1	1	0	PROM Auto Read Control XARD=0: enable auto read XARD=1: disable auto read
	1	0	0	0	0	XARD	0	0	0	0	
PROM Programming Control	0	0	1	0	0	1	1	0	0	0	PROM Programming Control EN=0 ; disable programming EN=1 ; enable programming
	1	0	0	0	0	EN	0	0	1	0	

9.4 INSTRUCTION DESCRIPTION (PROM Function)

9.4.1 Vop Increase

This instruction is used to increase Vop step by one (VOF[7:0]+1).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	0	

9.4.2 Vop Decrease

This instruction is used to decrease Vop step by one (VOF[7:0]-1).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	1	

9.4.3 Vop Offset

This instruction is changes VopOffset directly. It is not recommended to set VopOffset directly with this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	1	1	
1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	

9.4.4 PROM WR/RD Control

This instruction is used to set the status of PROM that write to PROM or read from PROM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	0	1	WR/RD=0: Enable PROM read RW/RD=1: Enable PROM write
1	0	0	0	WR /RD	0	0	0	0	0	

9.4.5 PROM Control Out

This instruction is used to cancel PROM control function.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	0	

9.4.6 PROM Write

This instruction is used to trigger PROM programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	1	

9.4.7 PROM Read

This instruction is used to trigger PROM up-load procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	0	0	

9.4.8 PROM Auto Read Control

This instruction is used to set status of PROM auto read function is enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	1	0	
1	0	0	0	0	XARD	0	0	0	0	

9.4.9 PROM Programming Control

This instruction is used to set status of PROM programming function is enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	1	0	0	0	PROM Programming Control EN=0 ; disable programming EN=1 ; enable programming
1	0	0	0	0	EN	0	0	1	0	

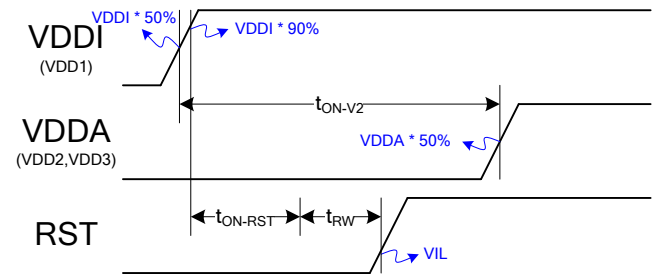
10 OPERATION FLOW

This section introduces some reference operation flows.

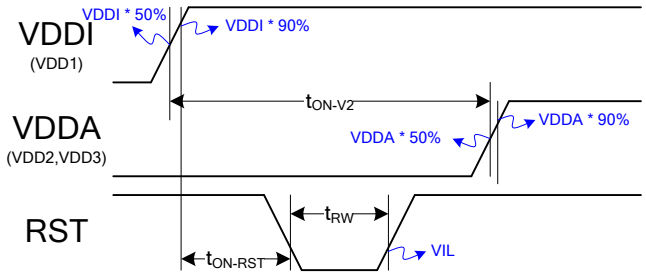
10.1 Power ON Flow

10.1.1 Power On Sequence

Case 1: RSTB=L while Power ON



Case 2: RSTB=H while Power ON



Note:

The detailed description can be found in the respective sections listed below.

1. Be sure the power is stable and the internal reset is finished (refer to RST timing specification).
2. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

Timing Requirement:

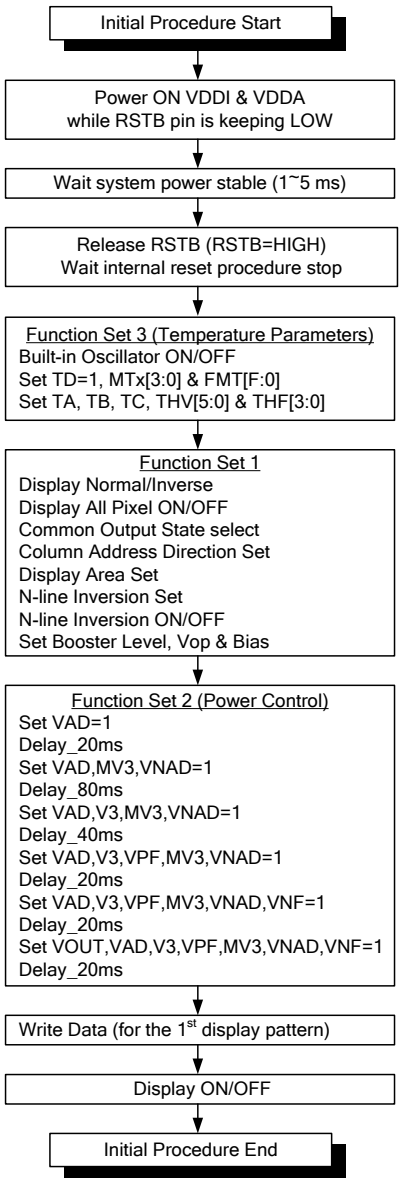
Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	● Applying VDDI and VDDA in any order will not damage IC.
RSTB input time	t_{ON-RST}	No Limitation	● If RST is Low, High or unstable during power ON, a successful hardware reset by RST is required after VDDI is stable. ● RST=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RST. ● To prevent abnormal display, the recommended timing is: $1ms \le t_{ON-RST} \le 30$ ms.

Note :

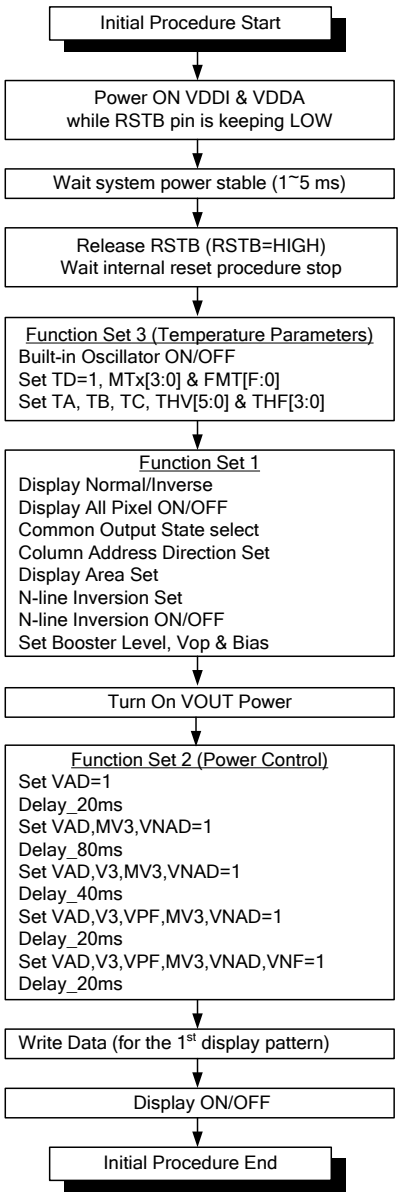
IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.

10.1.2 Referential Operation Flow

Internal Power Flow



External VOUT Flow



Note

1. The power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

10.1.3 Referential Initial Code

The following codes are listed for quick reference. Customer should fine tune parameters according to LCD performance.

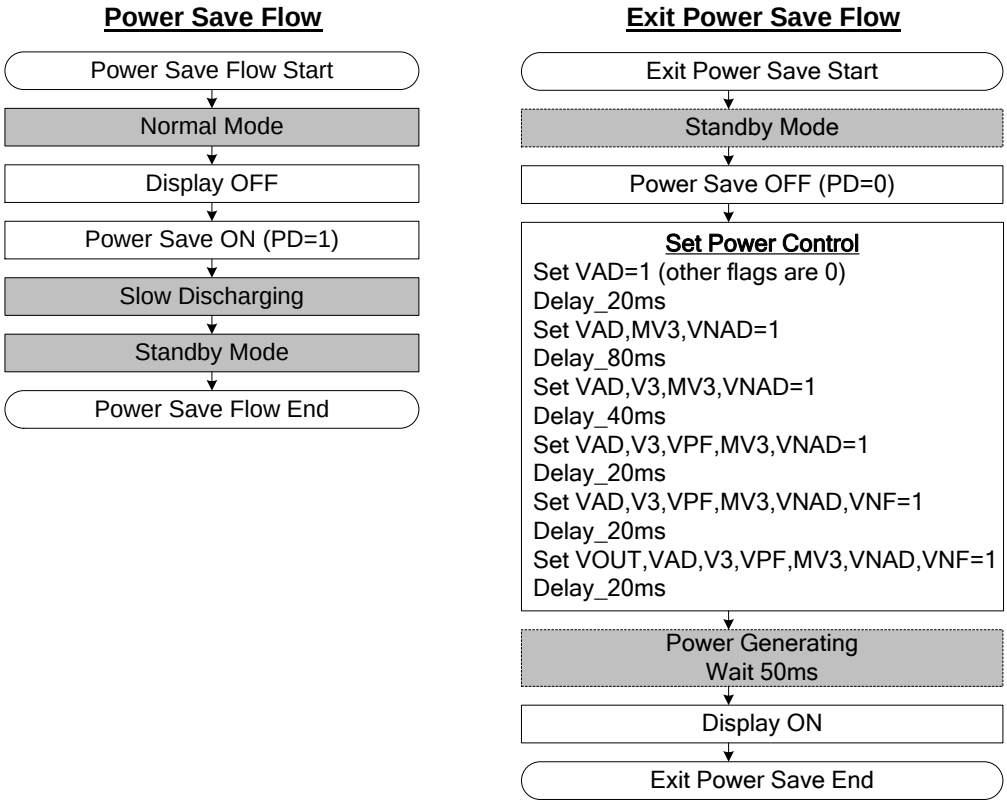
```
void initial(void)
{
  Reset_ms(1);
  Delay_ms(5);
  Write(COMMAND, 0xAE);          // Display OFF
  Write(COMMAND, 0xEA);          // Power Discharge Control
  Write(DATA, 0x00);             // Discharge OFF
  Write(COMMAND, 0xA8);          // Sleep-Out

// Start TC & OSC earlier for critical case with fast liquid crystal
  Write(COMMAND, 0xAB);          // OSC ON
  Write(COMMAND, 0x69);          // Temperature Detection ON
  Write(COMMAND, 0x4E);          // TC Setting
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(DATA, 0x00);             // 0mV/°C, should be adjusted by customer
  Write(COMMAND, 0x39);          // TC Flag
  Write(DATA, 0x00);
  Write(DATA, 0x00);
  Write(COMMAND, 0x2B)           //Frame Rate Level
  Write(DATA, 0x00)              //X1
  Write(COMMAND, 0x5F);          // Set Frame Frequency
  Write(DATA, 0x33);             // fFR=80Hz in all temperature range
  Write(DATA, 0x33);             // should be adjusted by customer
  Write(COMMAND, 0xEC);          // FR Compensation Temp. Range
  Write(DATA, 0x19);             // TA = -15 degree, should be adjusted by customer
  Write(DATA, 0x2D);             // TB = 5 degree, should be adjusted by customer
  Write(DATA, 0x55);             // TC = 45 degree, should be adjusted by customer
  Write(COMMAND, 0xED);          // Temp. Hysteresis Value (thermal sensitivity)
  Write(DATA, 0x04);             // Vop threshold: +2°C
  Write(DATA, 0x04);             // fFR threshold: +4°C
```

```
Write(COMMAND, 0xA6);       // Display Inverse OFF
Write(COMMAND, 0xA4);       // Disable Display All Pixel ON
Write(COMMAND, 0xC4);       // COM Output Status
Write(DATA, 0x02);          // Interlace mode, MY=0
Write(COMMAND, 0xA0);       // Column Address Direction: MX=0
Write(COMMAND, 0x6D);       // Display Area
Write(DATA, 0x07);          // Duty = 1/240 duty
Write(DATA, 0x00);          // Start Group = 1
Write(COMMAND, 0x84);       // Display Data Input Direction: Column
Write(COMMAND, 0x36);       // Set N-Line
Write(DATA, 0x08);          // N-Line=(8+1)x4=36
Write(COMMAND, 0xE4);       // N-Line OFF
Write(COMMAND, 0xE7);       // LCD Drive Method
Write(DATA, 0x19);          // NLFR=1
Write(COMMAND, 0x81);       // Set EV=64h
Write(DATA, 0x96);          // VOP=16V
Write(DATA, 0x00);
Write(COMMAND, 0xA2);       // BIAS
Write(DATA, 0x0A);          // 1/16 BIAS

Write(COMMAND, 0x25);       // Power Control
Write(DATA, 0x20);          // AVDD ON
Delay_ms(20);
Write(COMMAND, 0x25);       // Power Control
Write(DATA, 0x26);          // AVDD, MV3 & NAVDD ON
Delay_ms(80);
Write(COMMAND, 0x25);       // Power Control
Write(DATA, 0x36);          // AVDD, MV3, NAVDD & V3 ON
Delay_ms(40);
Write(COMMAND, 0x25);       // Power Control
Write(DATA, 0x3E);          // AVDD, MV3, NAVDD, V3 & VPF ON
Delay_ms(20);
Write(COMMAND, 0x25);       // Power Control
Write(DATA, 0x3F);          // AVDD, MV3, NAVDD, V3, VPF & VNF ON
Delay_ms(20);
Write(COMMAND, 0x25);       // Power Control
Write(DATA, 0x7F);          // VOUT, AVDD, MV3, NAVDD, V3, VPF & VNF ON
Delay_ms(20);

Write(COMMAND, 0xB1);       // Page Address
Write(DATA, 0x00);          // Page 0
```

```
  Write(COMMAND, 0x13);          // Column Address
  Write(DATA, 0x00);             // Start Column = 0
  Write(DATA, 0x00);
  Write(COMMAND, 0x1D);          // Write Data 9600 bytes to all DDRAM
  for(init i=0; i<9600; i++)
  Write(DATA, 0x00);             // Write Data 0x00 for 1st Display pattern

  Write(COMMAND, 0xAF);          // Display ON
}
```

10.2 Power Saving Flow

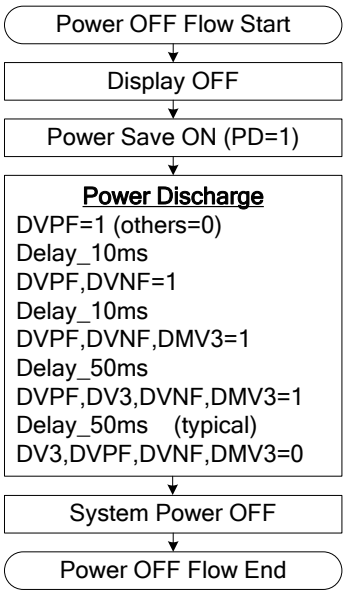
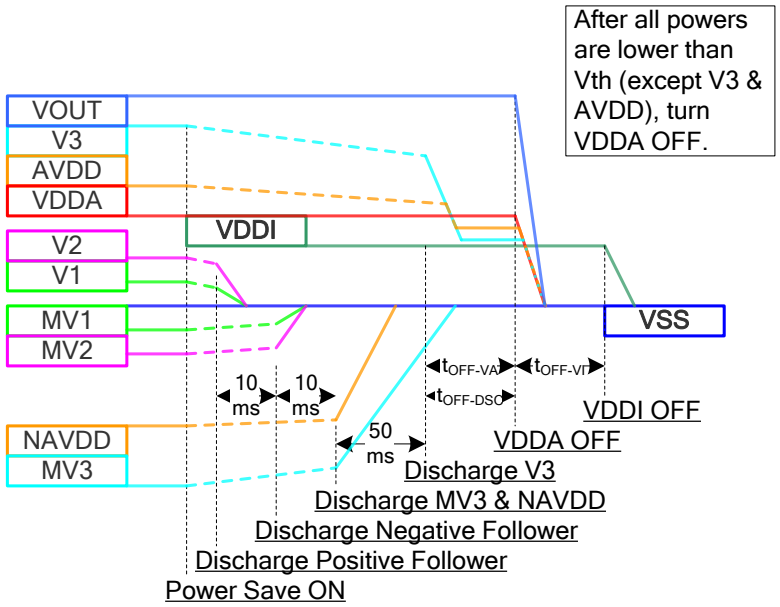
Referential Flow



Note: For external power application, please refer to the initial flow for the correct Power Control sequence.

10.3 Power OFF Flow

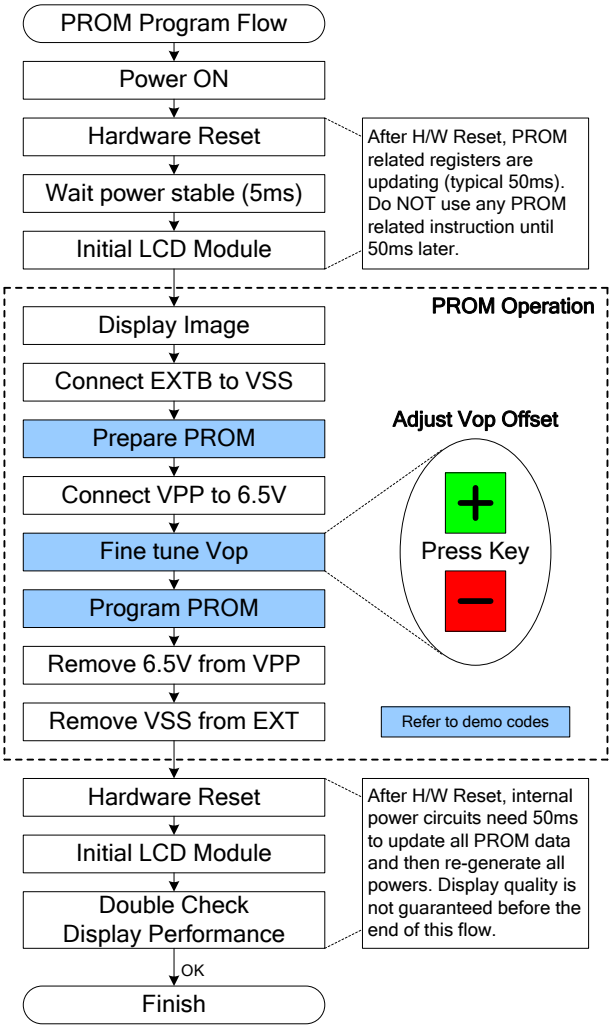
10.3.1 Power Off Sequence

Referential Operation Flow	Operation Sequence
	

Item	Symbol	Requirement	Description
Analog circuit discharge off delay	$t_{OFF-DSC}$	30ms ≤ $t_{OFF-DSC}$	● It is recommended to turn OFF analog discharge after the discharge procedure is finished. ● The discharge process is finished when: V2, V1, MV1 & MV2 are lower than Vth of liquid crystal; VDDA > AVDD > V3. ● The time will be different from LCD modules, since the panel loading & ITO resistance are different. And the system power and external capacitors will also influence it. ● The typical value is 50ms. And it is recommended to measure the time by real LCD module and application system.
VDDA power off delay	t_{OFF-VA}	$t_{OFF-DSC}$ ≤ t_{OFF-VA}	● Turn VDDA off after discharge procedure is finished. ● AVDD, VOUT and V3 fall as VDDA falling.
VDDI power off delay	t_{OFF-VI}	0 ≤ t_{OFF-VI}	● If VDDI and VDDA are separated, turn VDDI off after VDDA. ● The AVDD falling time depends on the LCD module and power circuit on the application system.

10.4 PROM Operation

10.4.1 Referential PROM Program Flow



Note:

1. If Vop is incorrect and display performance is not accepted after PROM programmed, please redo this flow again to fine tune Vop again.
2. Each press on the "+" or "-" key should execute one command 0xD6 (0xD7) to adjust VopOffset one step up (down).
3. Do not have the backlight closed to IC, because the temperature compensation is turned ON during the burning process. The backlight may heat IC and influence the altitude of Vop.
4. This flow (Burning Flow) is used for LCM assembler.
5. PROM can be written 3 times.

10.4.2 Referential PROM Operation Code

```
void PreparePROM (void)
{       //---------- Preset PROM mode before Programming PROM ----------
        Write(COMMAND, 0xFF);       // Enter PROM Test Mode
        Write(COMMAND, 0x98);       // Enable PROM Programming
        Write(DATA, 0x12);
        Write(COMMAND, 0x96);
        Write(DATA, 0x10);          // Disable Auto-Load
        Write(COMMAND, 0x94);       // Load Programmed data into Register
        Delay_ms(50);
        PROM_LED(ON);               // GPIO control LED ON
                                    // Reserved for PROM indicator of 6.5V switch (ON)
}

void FineTuneVop (void)
{       //---------- Fine tune Vop with "+" & "-" buttons ----------
      Write(COMMAND, 0xD6);         // Write command 0xD6 if "+" button is pressed
      or                            // Vop increase 1 step (VopOffset+1)
      Write(COMMAND, 0xD7);         // Write command 0xD7 if "-" button is pressed
                                    // Vop decrease 1 step (VopOffset-1)
}

void ProgramPROM (void)
{       //---------- Program PROM after VopOffset is adjusted ----------
      Write(COMMAND, 0x95);         // Program mode parameter
      Write(DATA, 0x08);
      Write(COMMAND, 0x91);         // Change PROM Control into Program mode
      Write(DATA, 0x20);
      Delay_ms(50);
      Write(COMMAND, 0x93);         // Program Start
      Delay_ms(300);
      Write(COMMAND, 0x92);         // Exit PROM control
      Write(COMMAND, 0x94);         // Load Programmed data into Register
      Delay_ms(50);
      Write(COMMAND, 0xFC);         // Exit PROM Test Mode
      PROM_LED(OFF);                // GPIO control LED OFF. Confirm display quality.
                                    // Reserved for PROM indicator of 6.5V switch (OFF)
}
```

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

12 ABSOLUTE MAXIMUM RATINGS

VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1 & VDD3)	–0.3 ~ 6.0	V
Analog Power supply voltage	VDDA (VDD2)	–0.3 ~ 6.0	V
LCD Power supply voltage	VOUT	–0.3 ~ 24	V
LCD Power supply voltage	V3	–0.3 ~ 16.5	V
LCD Power supply voltage	V2, V1	–0.3 ~ 6.0	V
LCD Power supply voltage	AVDD	–0.3 ~ 6.0	V
LCD Power supply voltage	NVDD	-6.0 ~ 0.3	V
LCD Power supply voltage	MV1, MV2	-6.0 ~ 0.3	V
LCD Power supply voltage	MV3	-16.5 ~ 0.3	V
MCU Interface Input Voltage	Vin	–0.3 ~ VDDI+0.3	V
MCU Interface Output Voltage	Vout	–0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	–40 to +85	°C
Storage temperature	TSTR	–55 to +105	°C

Note:

1. All voltages are respect to VSS1 unless otherwise noted (VSS1=VSS2=VSS3).
2. Stresses exceed the ranges listed above may cause permanent damage to IC.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Insure the voltage levels always match the correct relation (except Power ON and Power OFF sequence): VOUT > V3 > AVDD > V2 > V1 > VSS2 > MV1 > MV2 > NVDD > MV3
5. Stresses exceed the ABSOLUTE MAXIMUM RATINGS listed above may cause permanent damage to IC. These ratings are stress only. IC should be operated under DC/AC Characteristics condition for normal operation. If this condition is not met. IC operation may be error and the reliability may be deteriorated.

13 DC CHARACTERISTICS

VSS1=VSS2=VSS3 =0V and Ta = –40 ~ 85 °C, unless otherwise specified.

Item	Symbol	Condition	Related Pin	Rating			Unit
				Min.	Typ.	Max.	
Digital Operating Voltage	VDDI		VDD1, VDD3	2.7	–	5.5	V
Analog Operating Voltage	VDDA		VDD2	2.7	–	5.5	V
Input High-level Voltage	V_{IH}		MCU Interface	0.7*VDD1	–	VDD1	V
Input Low-level Voltage	V_{IL}		MCU Interface	VSS1	–	0.3*VDD1	V
Output High-level Voltage	V_{OH}	I_{OH}=1.0mA, VDD1=3V	D[7:0] TSYNC	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V_{OL}	I_{OL}=–1.0mA, VDD1=3V	D[7:0] TSYNC	VSS1	–	0.2*VDD1	V
V3 Accuracy	ΔV3	Ta=25°C, VDD=3.0V, V3=10V, Bias=1/12	V3	-0.12	–	0.12	V
Input Leakage Current	I_{IL}	Vin = VDD1 or VSS1	MCU Interface	–1.0	–	1.0	μA
ON Resistance of LCD Drivers	R_{ON}	Ta=25°C, Vop=20.0V, BIAS=1/15 ΔV=10%	COM Drivers	–	1	–	KΩ
		Ta=25°C, Vop=20.0V, BIAS=1/15 ΔV=10%	SEG Drivers	–	1	–	KΩ
Operation Clock	f_{OSC}	Ta = 25°C	–	–	275	–	KHz
Vop voltage output	Vop		V3-MV3	10	-	33	V
VOUT voltage output	VOUT		VOUT	-	18	20	V

The current consumed by whole IC (bare die) with internal power system:

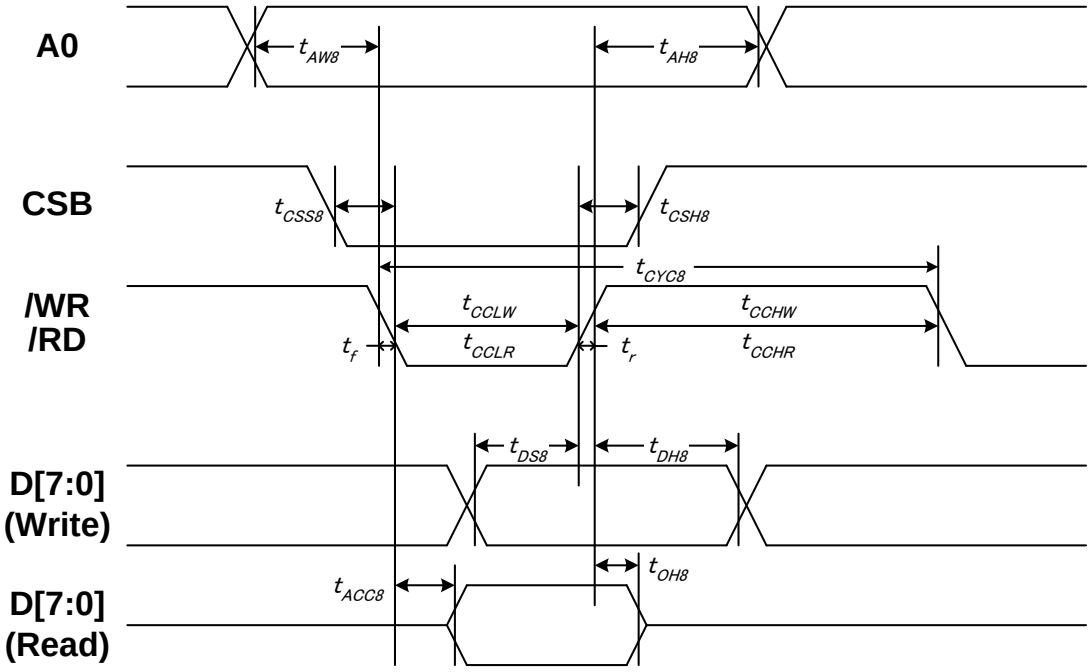
Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display Current	ISS	Display ON, Pattern: SNOW (Static), VDDI=VDDA=3.3V, Internal AVDD, Frame Rate Level=1, Vop = 20V, Bias=1/16, N-Line OFF, fFR=62Hz, Ta=25°C	–	4000	–	μA
Standby	ISS	VDDI=VDDA=3.3V, Internal AVDD, Ta=25°C	–	80	–	μA

Note:

The current is DC characteristic of a “Bare Chip”.

14 TIMING CHARATERISTIC

14.1 System Bus Timing for 8080 MCU Interface



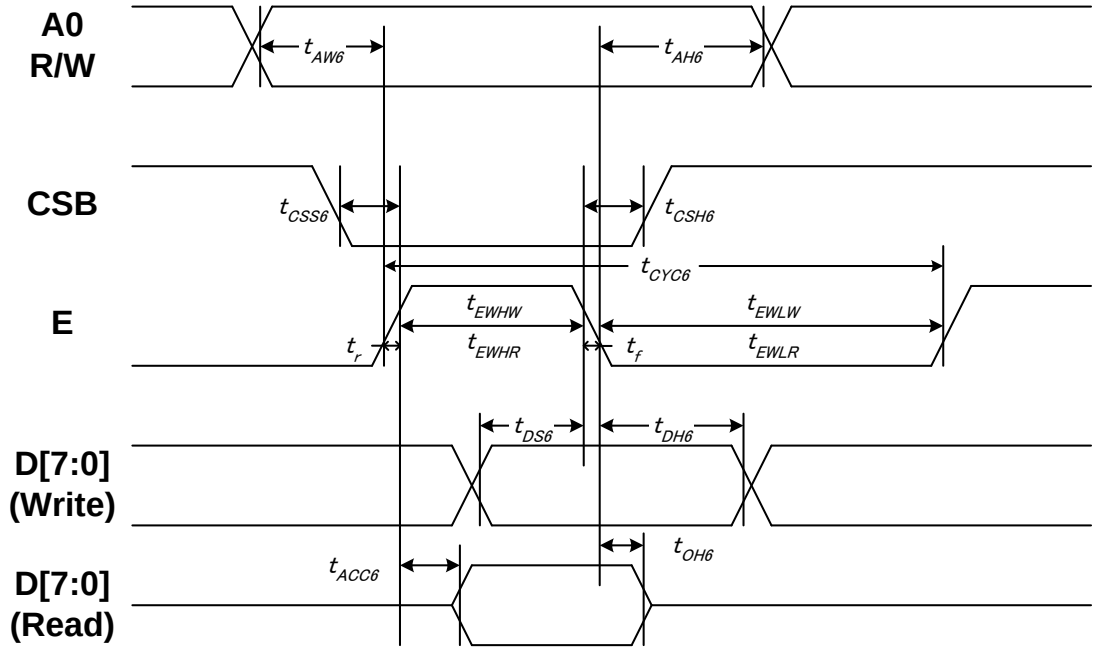
VDD1 = 3.0V~5.0V , Ta = –40 ~ 85 °C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		10	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		320	—	
/WR L pulse width (WRITE)		tCCLW		150	—	
/WR H pulse width (WRITE)		tCCHW		150	—	
/RD L pulse width (READ)	/RD	tCCLR		150	—	
/RD H pulse width (READ)		tCCHR		150	—	
CSB setup time	CSB	tCSS8		75	—	
CSB hold time		tCSH8		50	—	
WRITE Data setup time	D[7:0]	tDS8		50	—	
WRITE Data hold time		tDH8		50	—	
READ access time		tACC8	CL = 100 pF	—	100	
READ Output disable time		tOH8	CL = 100 pF		80	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level.
   CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns widther than /WR (or /RD).

14.2 System Bus Timing for 6800 MCU Interface



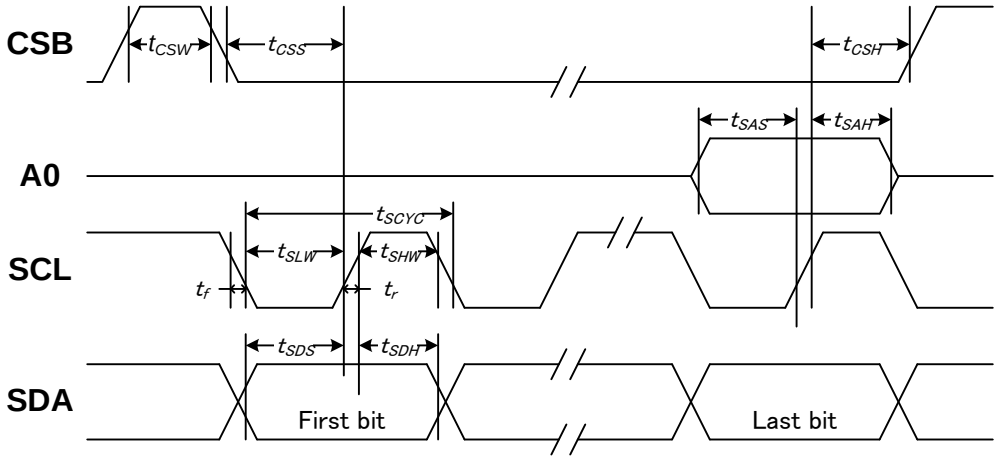
VDD1 = 3.0V~5.0V , Ta = –40 ~ 85 °C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		10	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		320	—	
Enable L pulse width (WRITE)		tEWLW		150	—	
Enable H pulse width (WRITE)		tEWHW		150	—	
Enable L pulse width (READ)		tEWLR		150	—	
Enable H pulse width (READ)		tEWHR		150	—	
CSB setup time	CSB	tCSS6		75		
CSB hold time		tCSH6		50		
Write data setup time	D[7:0]	tDS6		75	—	
Write data hold time		tDH6		50	—	
Read data access time		tACC6	CL = 100 pF	—	100	
Read data output disable time		tOH6	CL = 100 pF		90	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.
   CSB and E cannot act at the same time and CSB should be 100ns widther than E.

14.3 System Bus Timing for 4-Line SPI MCU Interface



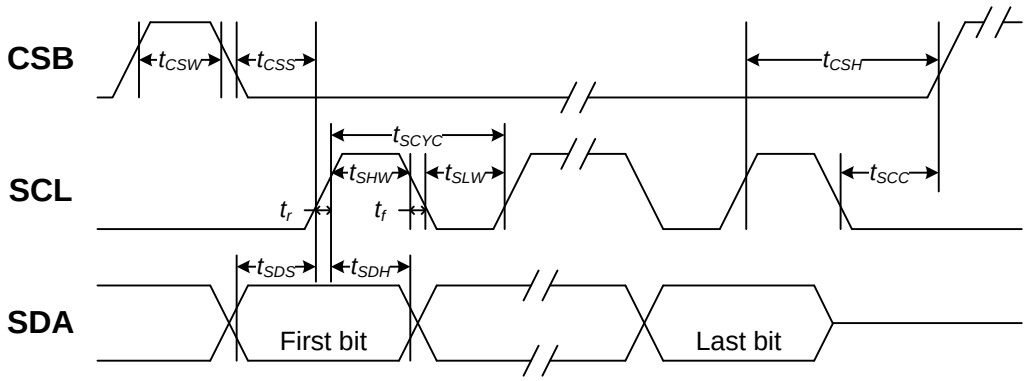
VDD1 = 3.0V~5.0V , Ta = –40 ~ 85 °C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		140	—	ns
SCL “H” pulse width		tSHW		70	—	
SCL “L” pulse width		tSLW		60	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		40	—	
Data hold time		tSDH		40	—	
CSB-SCL time	CSB	tCSS		60	—	
CSB-SCL time		tCSH		70	—	
CSB “H” pulse width		tCSW		15	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

14.4 System Bus Timing for 3-Line SPI MCU Interface



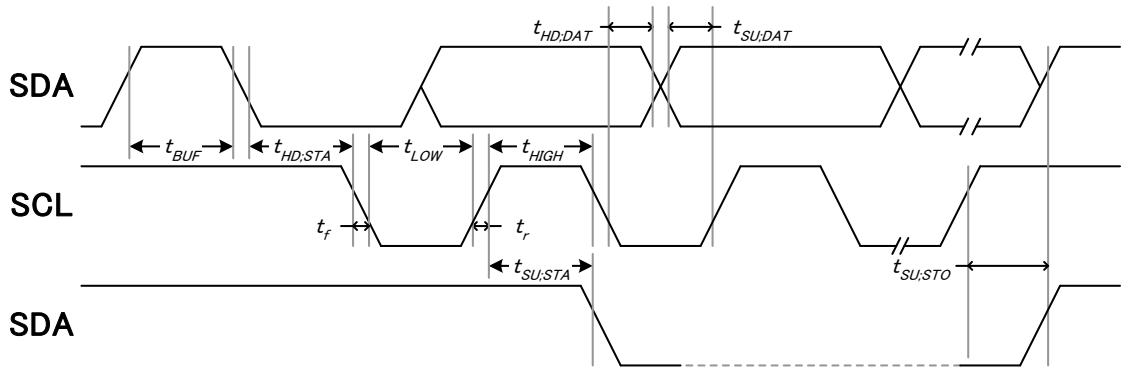
VDD1 = 3.0V~5.0V, Ta = –40 ~ 85 °C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Period	SCL	tSCYC		140	—	ns
SCL “H” pulse width		tSHW		70	—	
SCL “L” pulse width		tSLW		60	—	
SCL wait time		tSCC		40	—	
Data setup time	SDA	tSDS		40	—	
Data hold time		tSDH		60	—	
CSB-SCL time	CSB	tCSS		70	—	
CSB-SCL time		tCSH		15	—	
CSB “H” pulse width		tCSW		140	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard

14.5 System Bus Timing for I2C MCU Interface

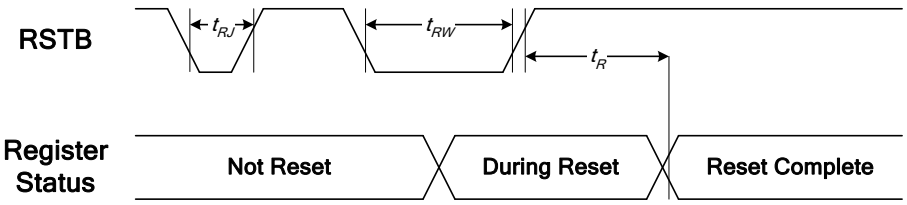


(VDD1 = 3.0V~5.0V, Ta = –40 ~ 85 °C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock frequency	SCL	fSCL		-	400	KHz
SCL clock LOW period		tLOW		1.3	-	us
SCL clock HIGH period		tHIGH		0.6	-	
BUS free time between a STOP and START		tBUF		1.3	-	
Data setup time	SDA	tSU;Data		0.1	-	
Data hold time		tHD;Data		0	0.9	
Setup time for a repeated START condition		tSU;STA		0.6	-	
Start condition hold time		tHD;STA		0.6	-	
Setup time for STOP condition		tSU;STO		0.6	-	
Signal rise time	SDA SCL	tr		20+0.1Cb	300	ns
Signal fall time		tf		20+0.1Cb	300	
Capacitive load represented by each bus line		Cb		-	400	pF
Tolerable spike width on bus		tSW		-	50	ns

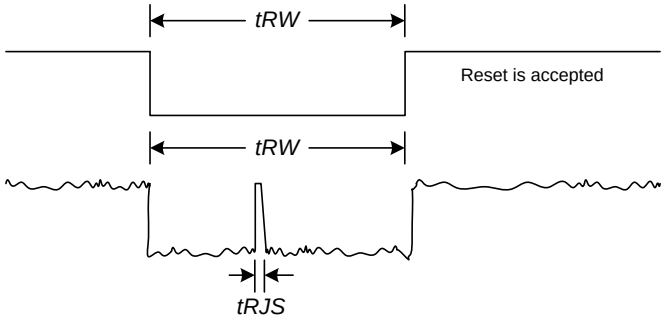
Note : All timing is specified using 20% and 80% of VDD1 as the standard.

14.6 Reset Timing



VDD1 = 3.0V~5.0V , Ta = –40 ~ 85 °C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	10 *1	us
Reset “L” pulse width		tRW		30	—	
Reset rejection		tRJ		—	10	
Reset rejection (for noise spike)		tRJS		—	20	ns

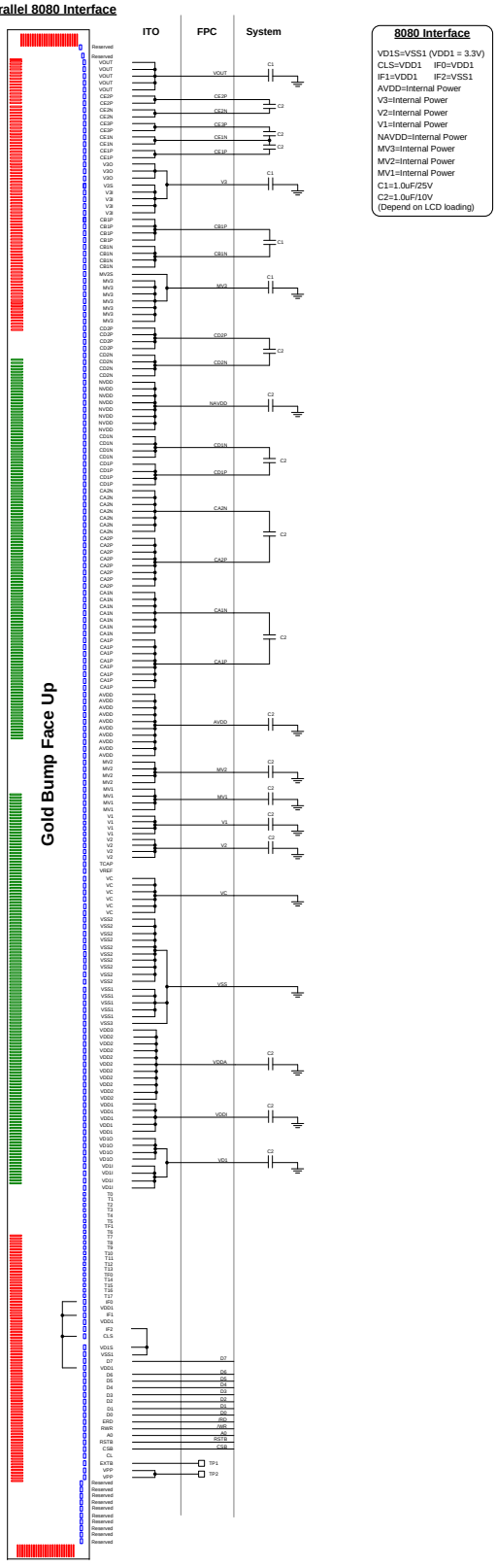


Note:

1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do NOT use any PROM related command during this period.
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than tRW specified above. If the LOW pulse is less than tRJ specified above, the reset procedure of IC will not start.
   If the LOW pulse is longer than tRJ and less than tRW, the reset procedure of IC is not guaranteed.

15 APPLICATION Circuit

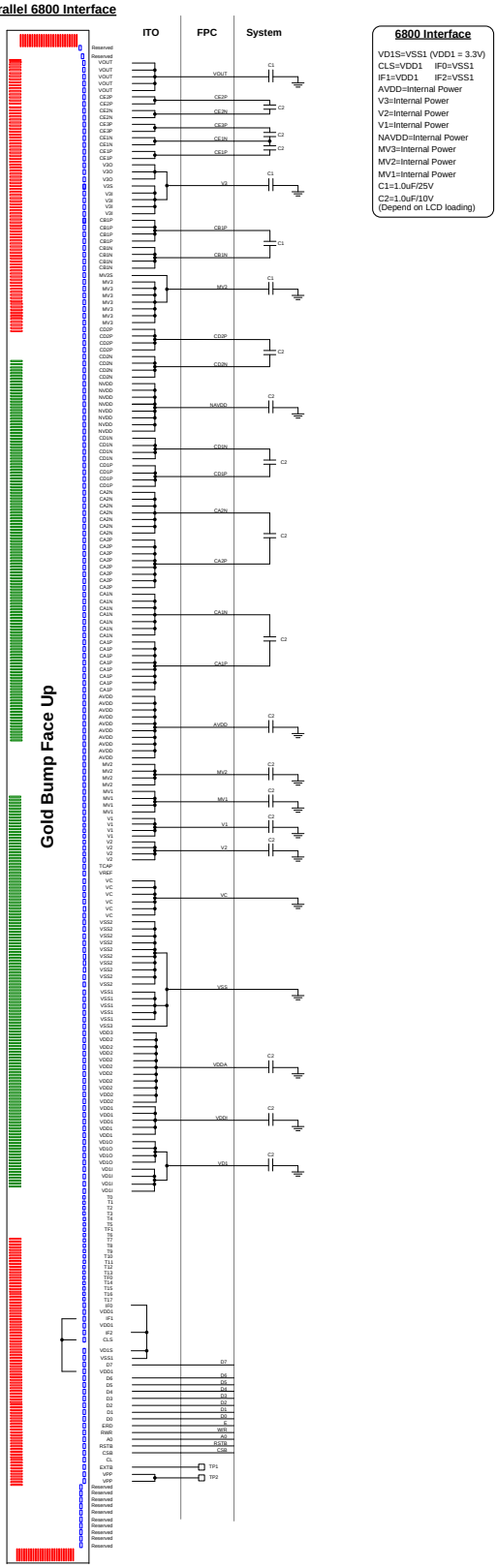
Parallel 8080 Interface



8080 Interface

VD1S=VSS1 (VDD1 = 3.3V)
CLS=VDD1 IF0=VDD1
IF1=VDD1 IF2=VSS1
AVDD=Internal Power
V3=Internal Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/25V
C2=1.0uF/10V
(Depend on LCD loading)

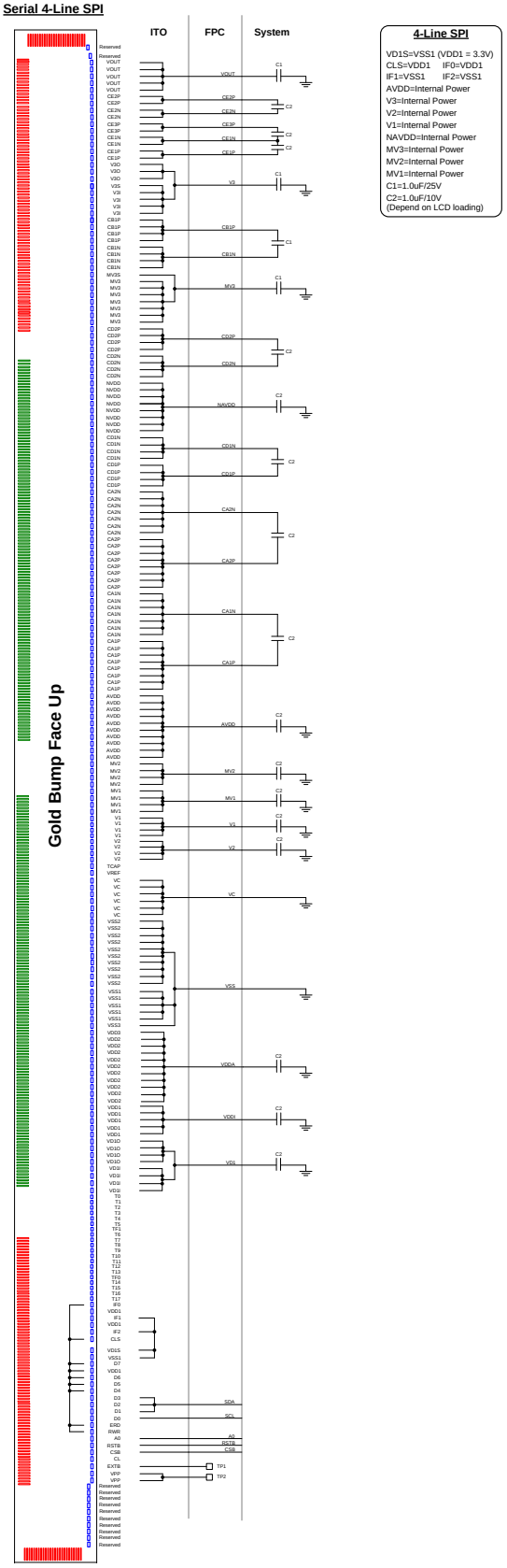
Parallel 6800 Interface



6800 Interface

VD1S=VSS1 (VDD1 = 3.3V)
CLS=VDD1 IF0=VSS1
IF1=VDD1 IF2=VSS1
AVDD=Internal Power
V3=Internal Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/25V
C2=1.0uF/10V
(Depend on LCD loading)

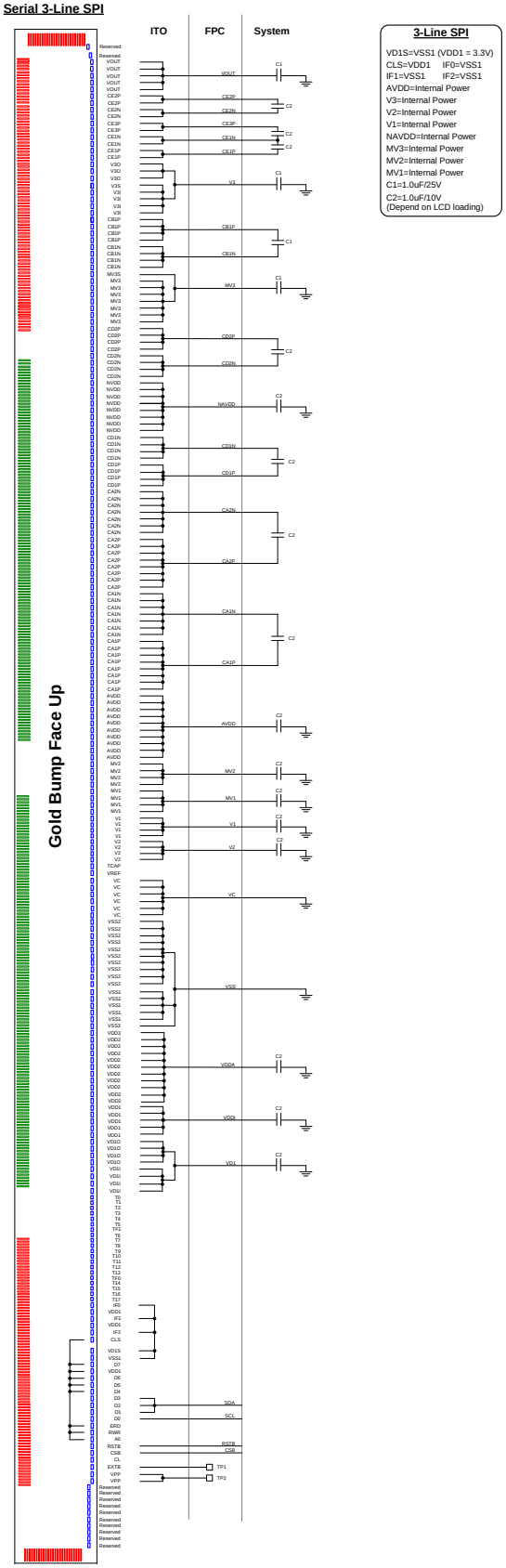
Serial 4-Line SPI



4-Line SPI

VD1S=VSS1 (VDD1 = 3.3V)
CLS=VDD1 IF0=VDD1
IF1=VSS1 IF2=VSS1
AVDD=Internal Power
V3=Internal Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/25V
C2=1.0uF/10V
(Depend on LCD loading)

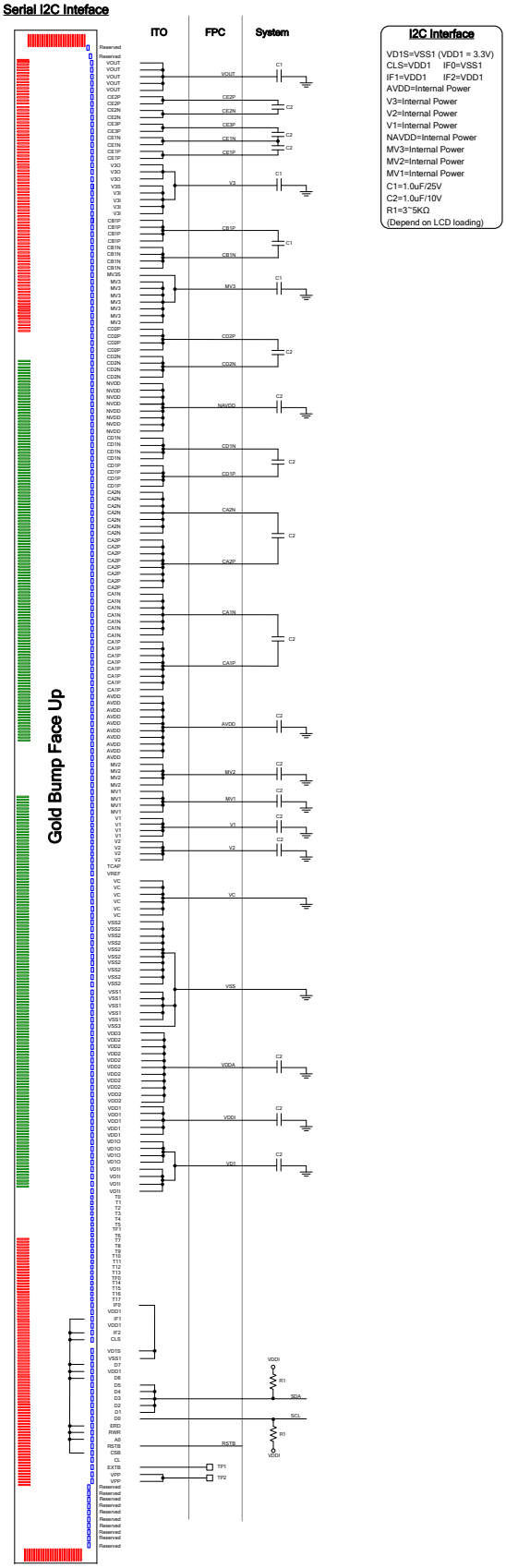
Serial 3-Line SPI



3-Line SPI

VD1S=VSS1 (VDD1 = 3.3V)
CLS=VDD1 IF0=VSS1
IF1=VSS1 IF2=VSS1
AVDD=Internal Power
V3=Internal Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/25V
C2=1.0uF/10V
(Depend on LCD loading)

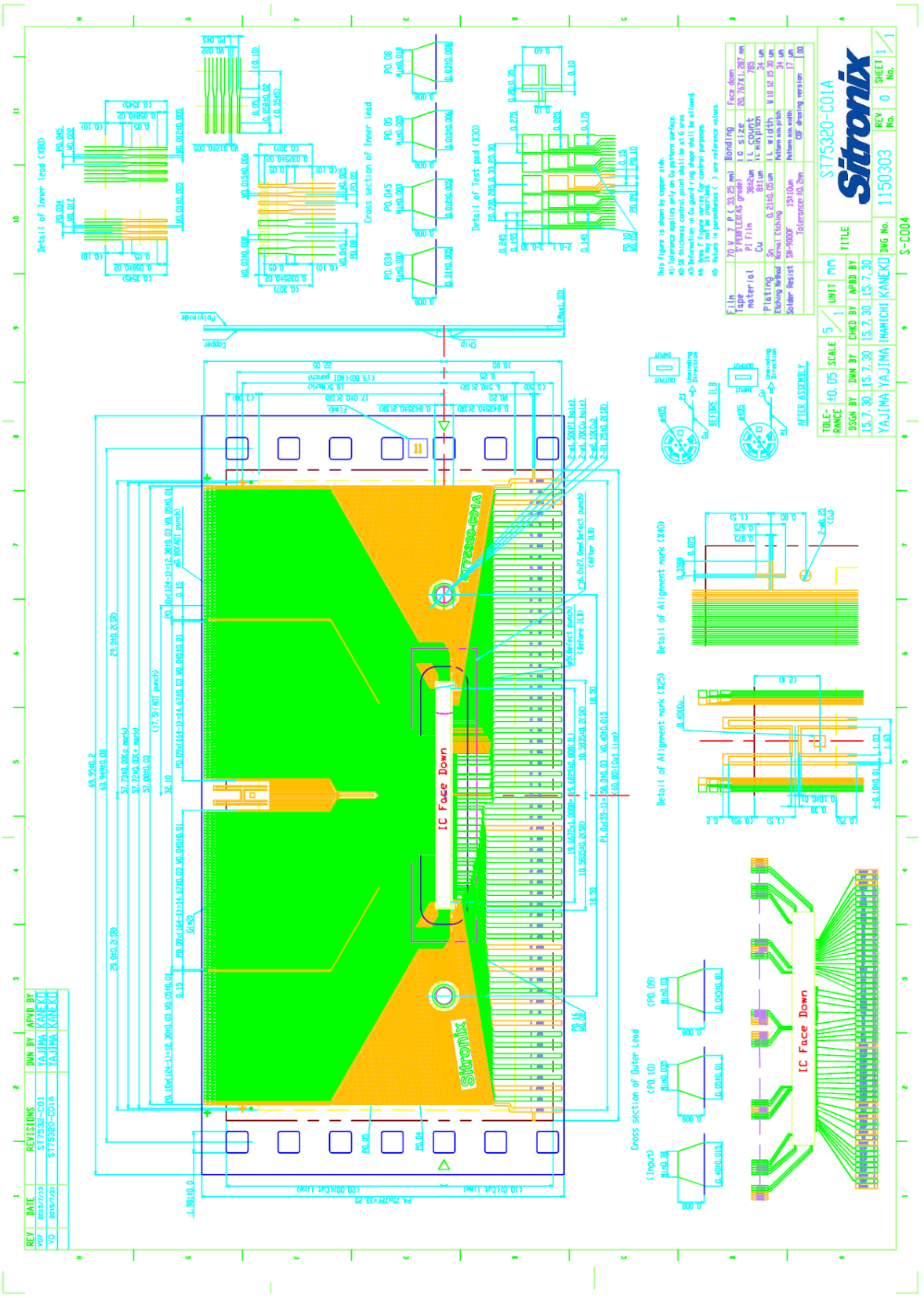
Serial I2C Inteface



I2C Interface

VD1S=VSS1 (VDD1 = 3.3V)
CLS=VDD1 IF0=VSS1
IF1=VDD1 IF2=VDD1
AVDD=Internal Power
V3=Internal Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/25V
C2=1.0uF/10V
R1=3~5KΩ
(Depend on LCD loading)

16 COF PACKAGE



17 REVERSION HISTORY

Version	Date	Description
0.1	2014/03/20	● Preliminary version.
0.2	2015/01/20	● Add Application Circuit. ● Modify Typing Error. ● Remove Gray Scale Setting. ● Remove Read DDRAM function. ● Add Read ID Instruction.
1.0	2015/04/28	● Formal Release
1.1	2015/07/14	● Modify Referential Initial Code ● Add PROM Programming Control Instruction ● Add COF PACKAGE